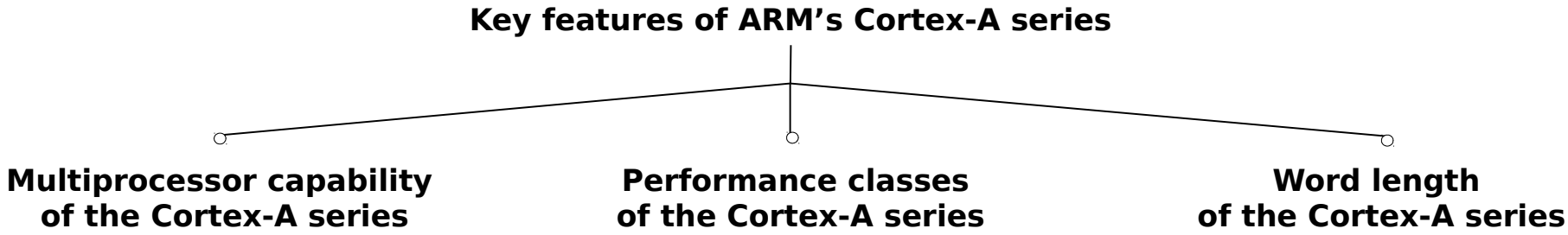
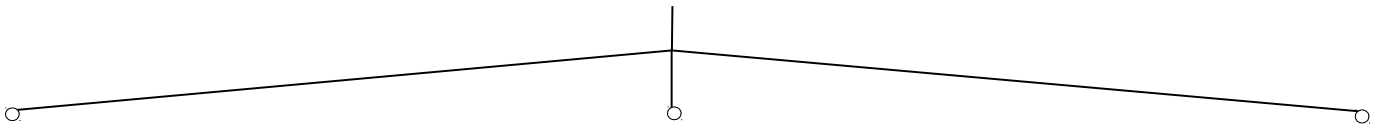
5. Overview of ARM’s Cortex-A series

5. Overview of ARM’s Cortex-A series

According to the general scope of this Lecture Notes, subsequently we will be concerned only with the Cortex-A series.



Multiprocessor capability of the Cortex-A series



Single processor designs, no multiprocessor capability

Cortex-A8 (2005)

Dual designs with two options

- **a single processor option and**
- **a multiprocesor capable option**

Cortex-A9/Cortex-A9 MPCore (2007)
Cortex-A12/Cortex-A12 MPCore (2013)
Cortex-A15/Cortex-A15 MPCore (2010)
Cortex-A17/Cortex-A17 MPCore (2014)

A-priory multiprocessor designs

Cortex-A7 MPCore (2011)
Cortex-A35 (2015)
Cortex-A53 (2012)
Cortex-A57 (2012)
Cortex-A72 (2015)

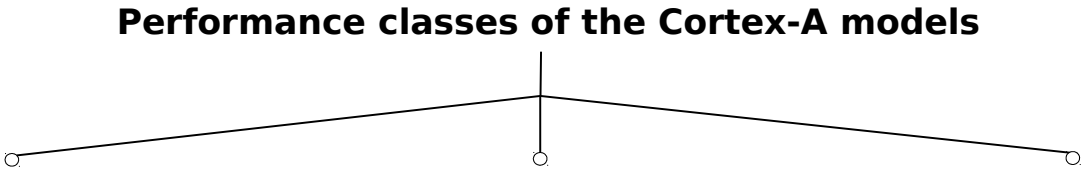
Here we note that in figures or tables we often omit the MPCore tag for the sake of brevity.

5. Overview of ARM's Cortex-A series (3)

Remarks on the interpretation of the term MPCore by ARM

- ARM introduced the term MPCore in connection with the announcement of the ARM11 MPCore in 2004 and interpreted it as multicore implementation (actually including up to 4 cores).
- Along with the ARM Cortex-A9 MPCore ARM re-interpreted this term such that it indicates now the multiprocessor capability of the processor.

Performance classes of the Cortex-A series -1 [12]



High-performance models	Mainstream models	Low-power models
Cortex-A15	Cortex-A8	Cortex-A5
Cortex-A57	Cortex-A9	Cortex-A7
Cortex-A72	(Cortex-A12)	Cortex-A35
	Cortex-A17	Cortex-A53

5. Overview of ARM’s Cortex-A series (6)

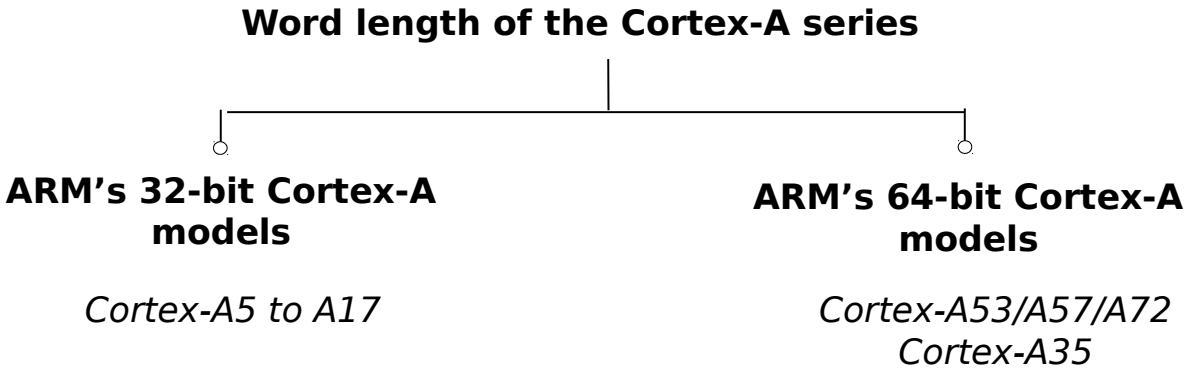
Announcement dates and efficiency (DMIPS/MHz) of the Cortex-A models

Announced	Cortex-A model	DMIPS/MHz
10/2005	Cortex-A8	2.0
	C	

Source: ARM

DMIPS: Dhrystone MIPS (A synthetic benchmark that indicates integer performance)

Word length of the Cortex-A series



5. Overview of ARM's Cortex-A series (9)

Key features of ARM's 32-bit microarchitectures -1 (based on [14])

2014 (Enhanced A12)	Cortex-A17	2-wide	2 decode	Out-of-Order issue; Pipeline; Up to 6; Pipeline; 11+ Stages	1-4 cores	3.1-3.3 DMIPS/MHz 2+ GHz 28nm
2010	Cortex-A15	2-wide	3 decode	Out-of-Order issue; Pipeline; Up to 8; Pipeline; 15+ Stages	1-4 cores	3.5-4.0 DMIPS/MHz 2+ GHz 32/28/22nm
2013	Cortex-A12	2-wide	2 decode	Out-of-Order issue; Pipeline; Up to 7; Pipeline; 11+ Stages	1-4 cores	3.0 DMIPS/MHz 2+ GHz 28nm
2007	Cortex-A9	2-wide	2 decode	Out-of-Order issue; Pipeline; Up to 9; Pipeline; 9-12 Stages	1-4 cores	2.5 DMIPS/MHz 2+ GHz 45/40/32/28nm
2005	Cortex-A8	2-wide	2 decode	In-Order; Pipeline; Up to 11; Pipeline; 13 Stages	1 core	2 DMIPS/MHz 1 GHz 65/45nm
2011	Cortex-A7	2-wide	2 decode	In-Order; Pipeline; Up to 5; Pipeline; 8 Stages	1-4 cores	1.9 DMIPS/MHz 1.7 GHz 28nm
2009 (A9 replacement for low-end devices)	Cortex-A5	1-wide	1 decode	In-Order; Pipeline; Up to 4; Pipeline; 9 Stages	1-4 cores	1.6 DMIPS/MHz 1 GHz 28nm

5. Overview of ARM's Cortex-A series (10)

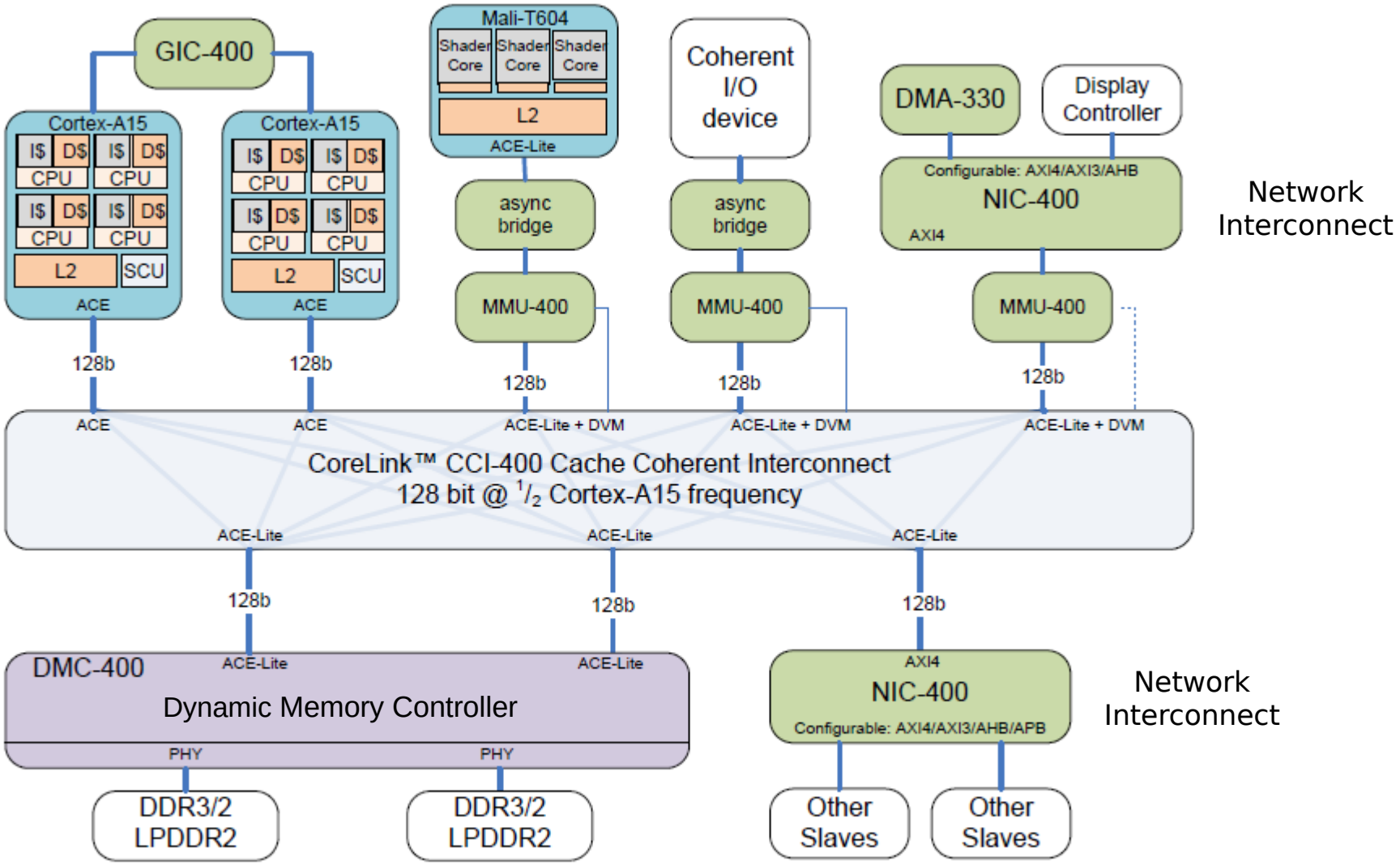
Key features of ARM's 64-bit microarchitectures -2 (based on [14])

64-bit

2013	Cortex-A57	3-wide	3 decode, Out-of-Order issue, Pipeline, Up to 8, 15+ Stages, Pipeline	1-4 cores	4.1-4.7 DMIPS/MHz 1.5-2.5 GHz 20/16 nm
2013	Cortex-A53	2-wide	2 decode, In-Order, Pipeline, Up to 5, 8 Stages, Pipeline	1-4 cores	2.3 DMIPS/MHz 1.2+ GHz 28/20 nm
2015	Cortex-A72	3-wide	3 decode, In-Order, Pipeline, Up to 8, 15+ Stages, Pipeline	1-4 cores	6.3-7.35 DMIPS/MHz 2.5 GHz 16 nm
2015	Cortex-A35	2-wide	2 decode, In-Order, Pipeline, Up to n.a., 8 Stages, Pipeline	1-4 cores	~2.1 DMIPS/MHz 1+ GHz 28/16/14 nm

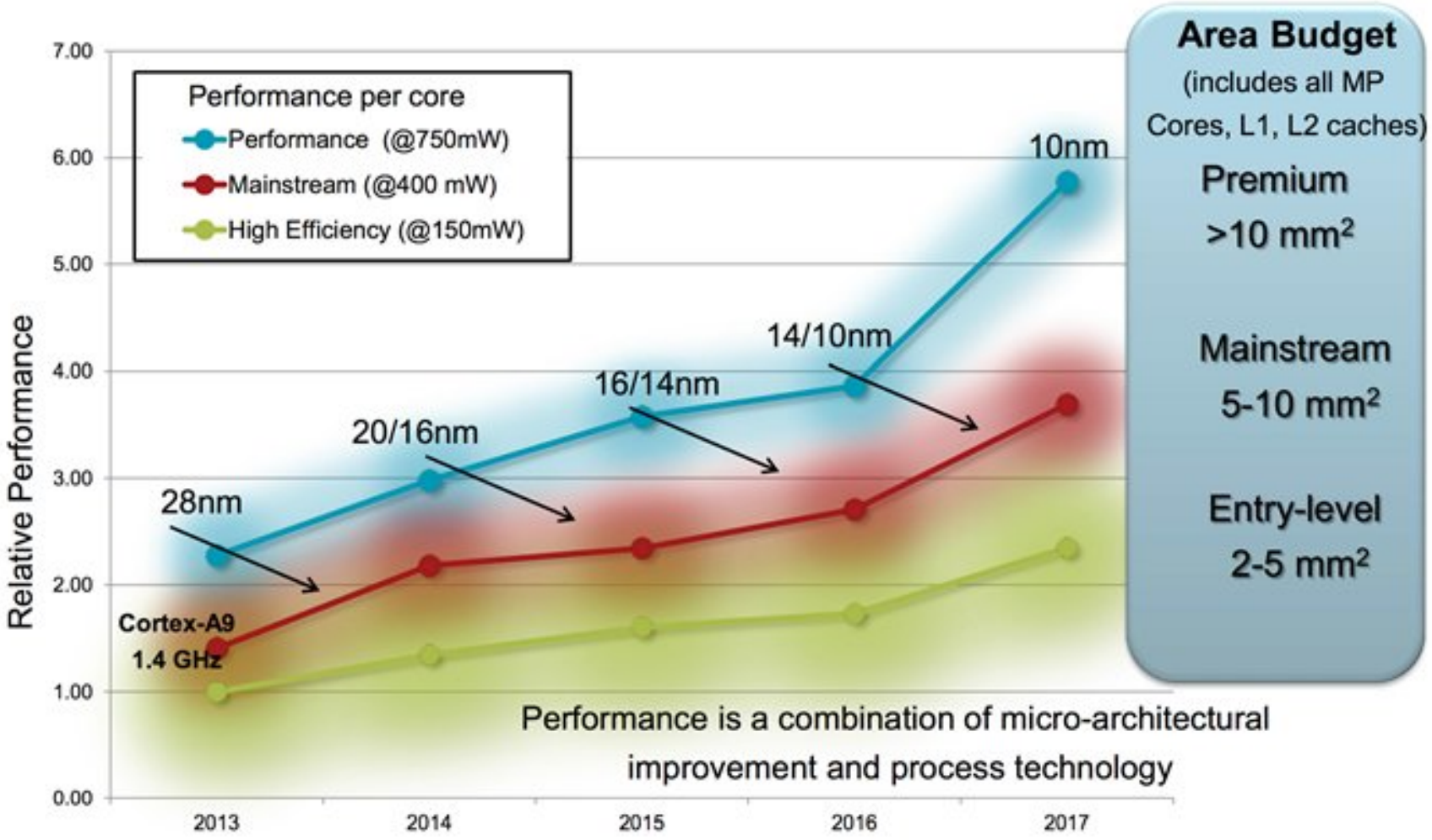
Remark: In the Cortex-A9 the NEON FP operates in order.

Example: Dual-core A15-based high performance cache coherent system [15]



5. Overview of ARM's Cortex-A series (12)

Relative per core performance of Cortex-A processors with different power budget [16]



5. Overview of ARM's Cortex-A series (14)

Use of 32-bit ARM Cortex-A models in mobiles [18]

	(SOC) System-On-a-Chip	Notable Product(s) Containing	ARM Cortex-A model	No. of Cores
Apple	**A4**	iPhone 4, iPod Touch (4th Gen), iPad (1st Gen), AppleTV (2nd Gen)	Cortex-A8	1
	A5	iPhone 4S, iPad 2, AppleTV (3rd Gen)	Cortex-A9	2
	A5X	iPad (3rd Gen, Retina Display)	Cortex-A9	2
Samsung	**Exynos 3 Single**	Samsung Galaxy S, Samsung Galaxy Nexus S,	Cortex-A8	1
	Exynos 4 Dual	Samsung Galaxy SII, Samsung Galaxy Note (International)	Cortex-A9	2
	Exynos 4 Quad	Samsung Galaxy SIII	Cortex-A9	4
	Exynos 5 Dual	Chrombook	Cortex-A15	2
Nvidia	**Tegra**	Microsoft Zune HD	(ARM11)	1
	Tegra 2	ASUS Eee Pad Transformer, Samsung Galaxy Tab 10.1, Motorola Xoom, Dell Streak 7 & Pro, Sony Tablet S	Cortex-A9	2
	Tegra 3	ASUS Transformer Pad 300, ASUS Nexus 7, Acer Iconia Tab A510 & A700, HTC One X	Cortex-A9	4
Qualcomm	**Snapdragon S1**	Large number of devices	(ARM11)/A5	1
Texas Instruments	**OMAP 3**	Barnes and Noble Nook Color	Cortex-A8	1
	OMAP 4	Amazon Kindle Fire, Samsung Galaxy Tab 2, Blackberry Playbook, Samsung Galaxy Nexus, Barnes and Noble Nook Tablet	Cortex-A9	2
	OMAP 5	N/A	Cortex-A15	2

7. The 64-bit Cortex-A series

- 7.1 Overview of ARM’s 64-bit Cortex-A series
- 7.2 The 64-bit high performance Cortex-A57
- 7.3 The 64-bit low power Cortex-A53

7.1 Overview of ARM’s 64-bit Cortex-A series

7.1 Overview of ARM's 64-bit Cortex-A series -1 [64]

10/2011 ARM disclosed the 64-bit ARMv8 architecture with enhancements as indicated in the Figure below and discussed in Section 2.

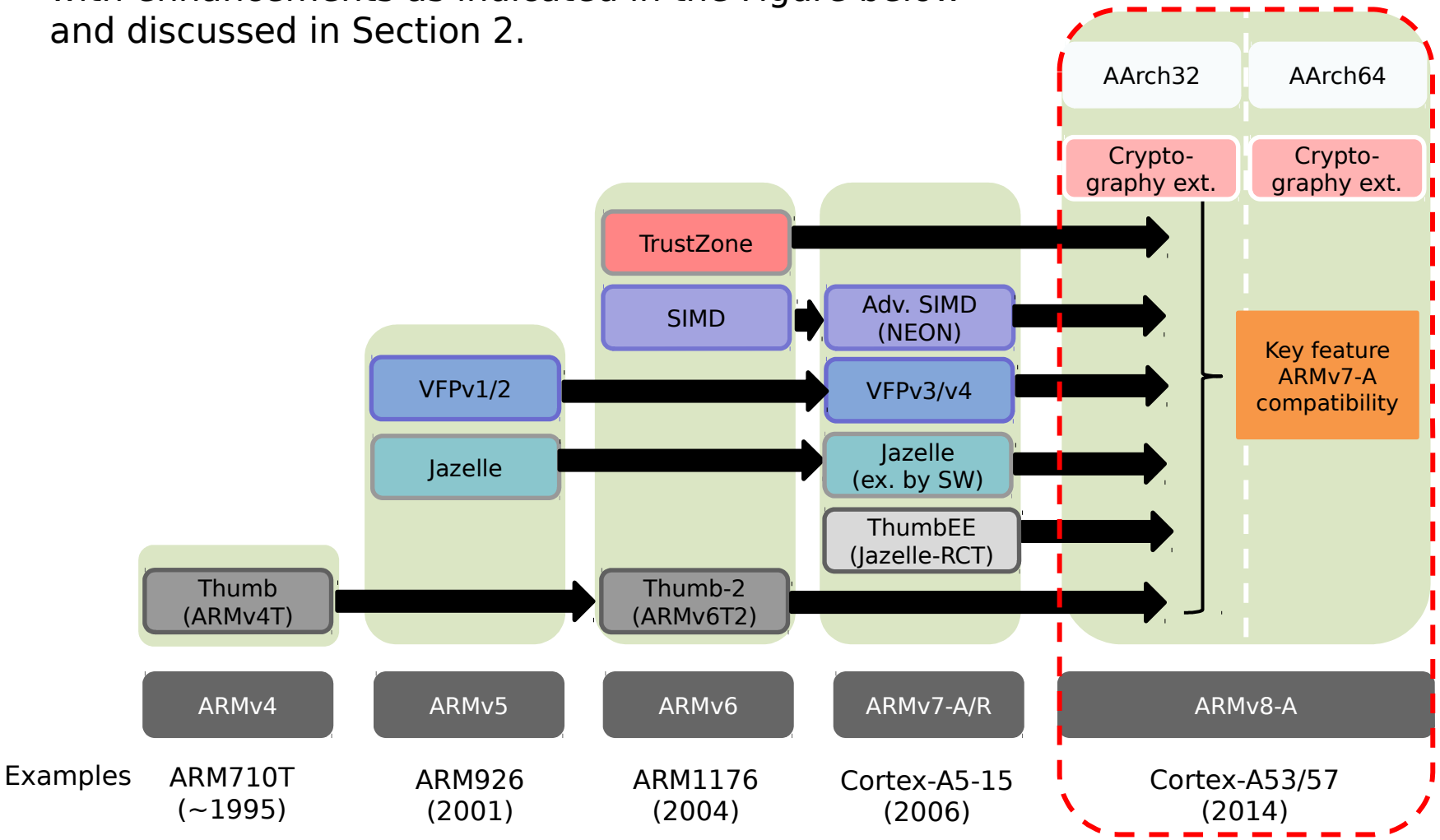
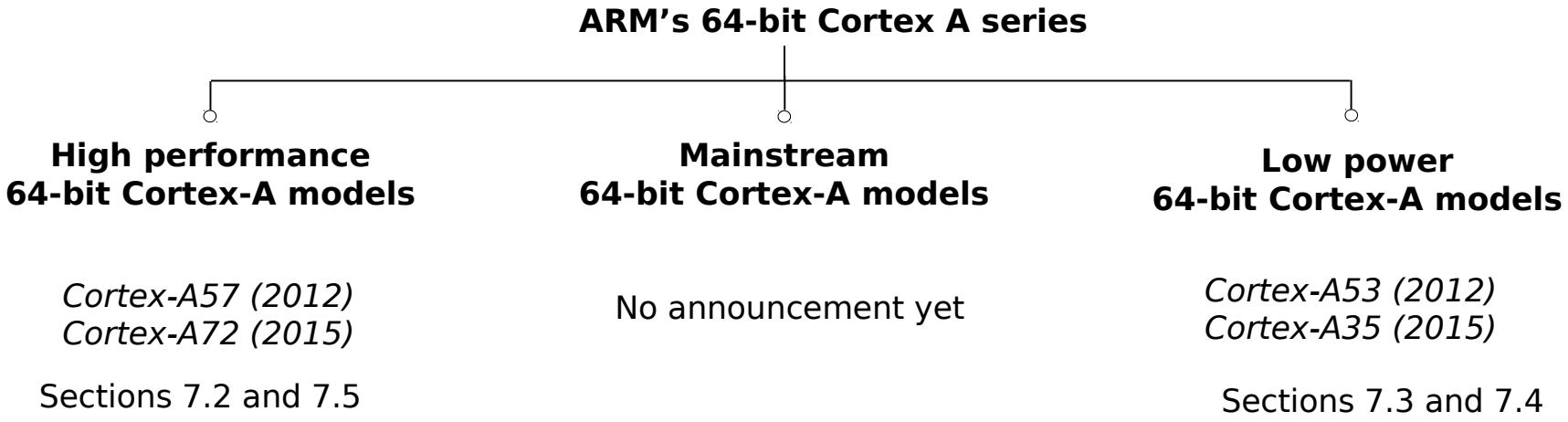


Figure: Enhancements of the ARM architecture (based on [64])

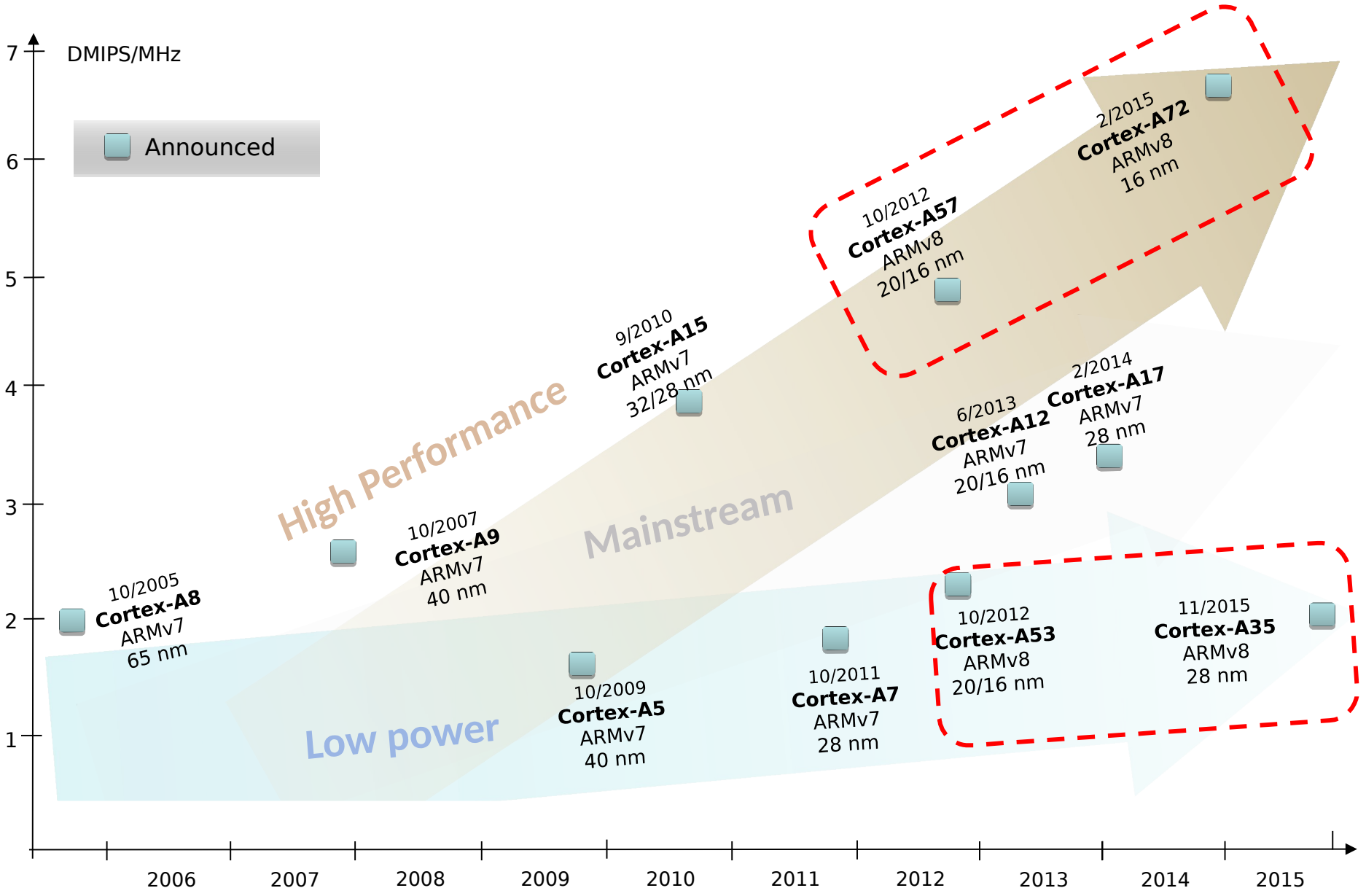
Overview of ARM's 64-bit Cortex-A series -2

- 10/2012: ARM announced the 64-bit high performance Cortex-A-57 and the low power Cortex-A-53 processors, as first implementations of the ARMv8 architecture, with immediate availability.
- 02/2015 ARM extended their 64-bit Cortex-A series by the high performance Cortex-A72 model, and then in
- 11/2015 with the 64-bit low power Cortex-A35, as shown below.



5. Overview of ARM's Cortex-A series (6)

Overview or ARM's 64-bit Cortex-A series -3 (based on [12])



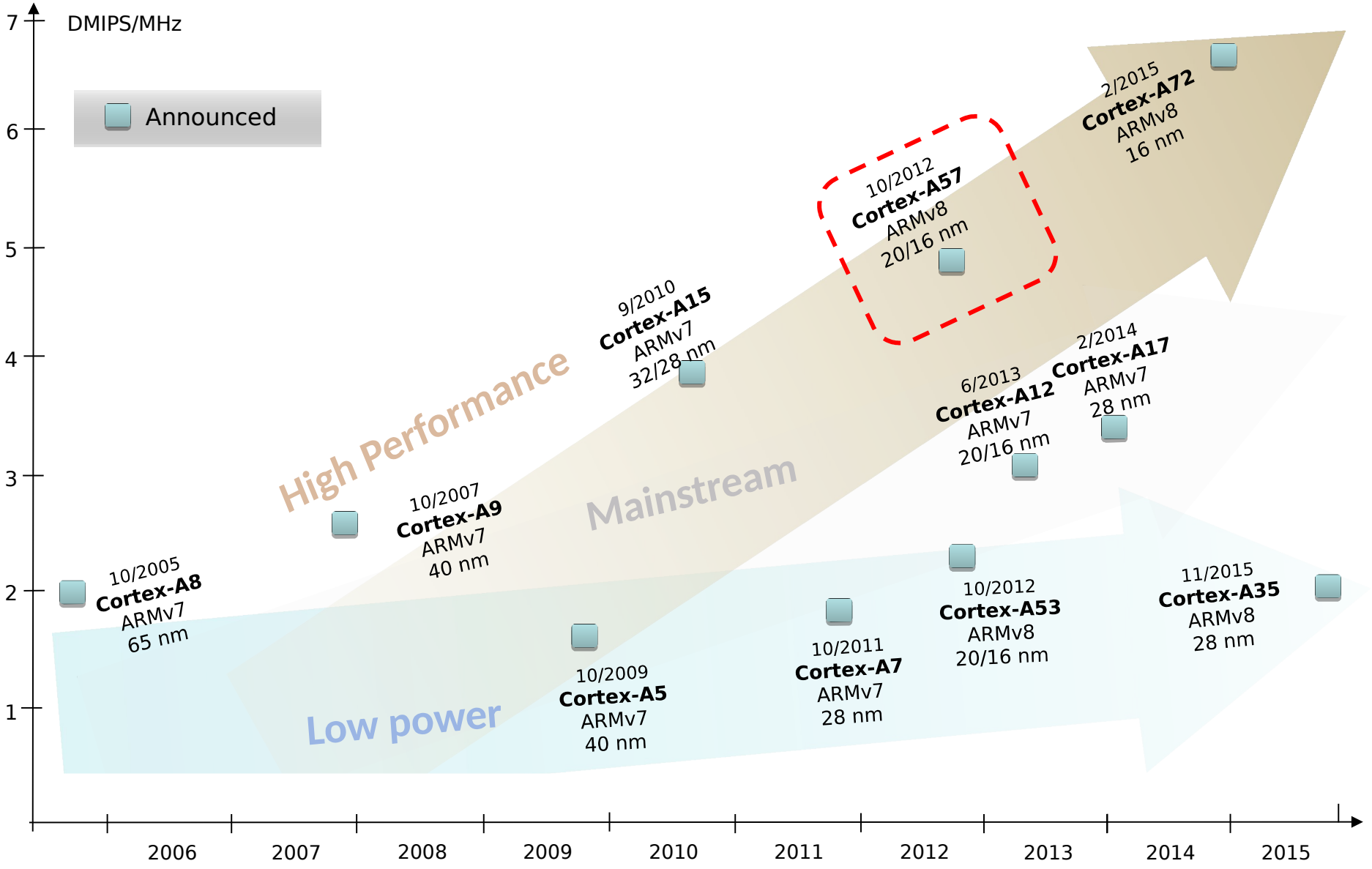
7.1 Overview of ARM's 64-bit Cortex-A series (6)

Main features of ARM's 64-bit Cortex-A series [51]

CPU Core	Architecture	Efficiency	big.LITTLE	Announced	Available in devices	Target
Cortex-A72	ARMv8 (64-bit)	6.3-7.3 DMIPS/MHz	Yes (with A53/A35)	2015	n.a.	High-end
Cortex-A57	ARMv8 (64-bit)	4,8 DMIPS/MHz	Yes (with A53)	2012	2015	High-end
Cortex-A53	ARMv8 (64-bit)	2,3 DMIPS/MHz	Yes (with A57)	2012	2H 2014	Low power
Cortex-A35	ARMv8 (64-bit)	2,1 DMIPS/MHz	Yes (with A57/A72)	2015	2H 2016	Low power
Cortex-A17	ARMv7 (32-bit)	4,0 DMIPS/MHz	Yes (with A7)	2014	2015	Mainstream
Cortex-A15	ARMv7 (32-bit)	4,0 DMIPS/MHz	Yes (with A7)	2010	Now	High-end
Cortex-A12	ARMv7 (32-bit)	3,0 DMIPS/MHz	-	2013	2H 2015	Mainstream
Cortex-A9	ARMv7 (32-bit)	2,5 DMIPS/MHz	-	2007	Now (EOL)	High-end
Cortex-A8	ARMv7 (32-bit)	2,0 DMIPS/MHz	-	2005	Now (EOL)	High-end
Cortex-A7	ARMv7 (32-bit)	1,9 DMIPS/MHz	Yes (A15/A17)	2011	Now	Low power
Cortex-A5	ARMv7 (32-bit)	1,6 DMIPS/MHz	-	2009	Now	Low power

7.2 The 64-bit high performance Cortex-A57

7.2 The 64-bit high performance Cortex-A57 -1 (based on [12])



7.2 The 64-bit high performance Cortex-A57 (2)

The 64-bit high performance Cortex-A57 -2 [12]

- 10/2012: Announced along with the low power Cortex-A53 processor, with immediate availability for licensing.
- 2014: First mobile devices with Cortex-A57 models are emerged.
- They are 64-bit successors to the high performance 32-bit Cortex A15.
- The A57 and A53 models can be used either as stand alone processors or as components of a big-LITTLE configuration, similar to the 32-bit Cortex-A15/A7 combination.
- Interoperability with the ARM Mali GPU family is provided.
- Target process technology: 16 or 20 nm.

7.2 The 64-bit high performance Cortex-A57 (3)

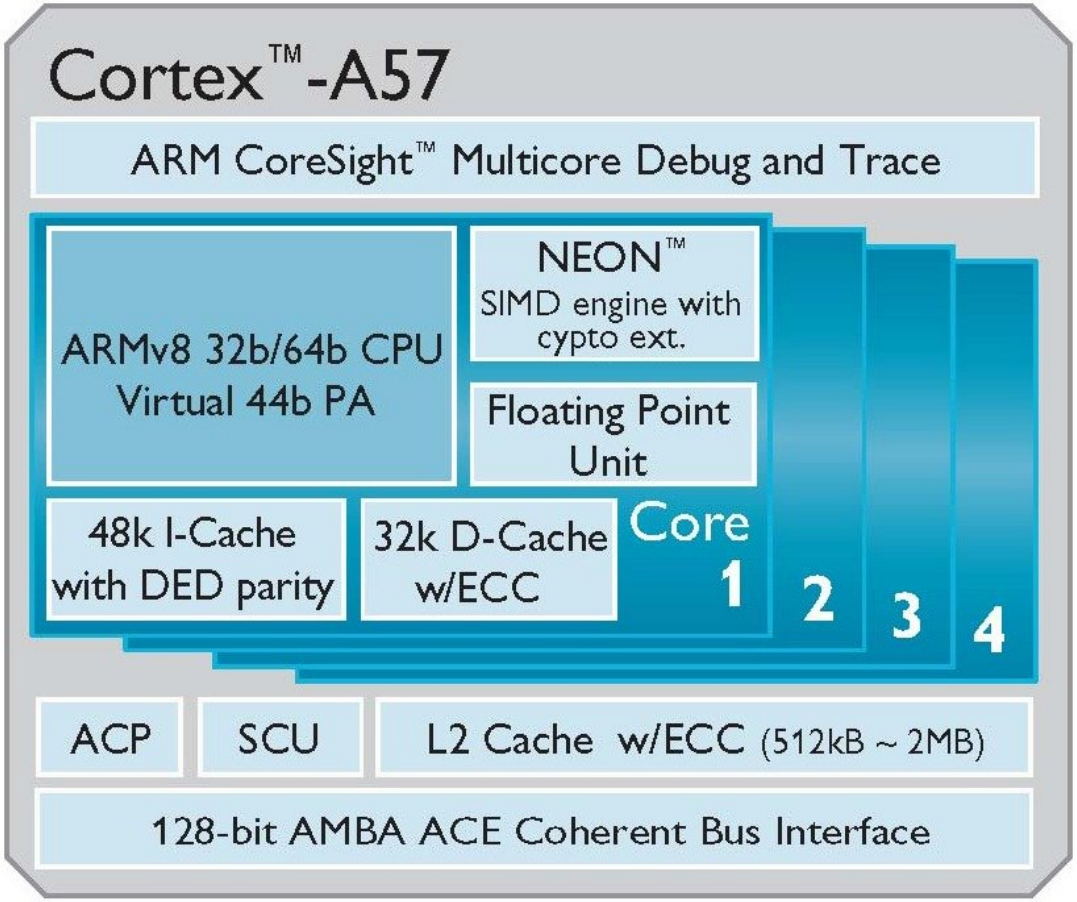
Key features of the Cortex-A57

- Fully compatible with the preceding ARMv7 32-bit ISA.
- Integrated L2 cache of 512 kB to 2 MB.
- Up to 4 Cortex-A57 CPUs that execute the ARMv8 64-bit ISA.
- 128-bit AMBA coherent interface for connecting multiple (up to 4) Cortex-A57 processors.
- System wide cache coherence supported by a Snoop Control Unit (SCU).

Remarks

AMBA: Advanced Microcontroller Bus Architecture
(On-chip bus standard for SoC) designs

High level block diagram of the Cortex-A57 [53]



PA: Physical Address

DED: Double Error Detection

ECC: Error Correcting Code

ACP: Accelerator Coherence Port
(to connect non-cached coherent data sources)

SCU: Snoop Control Unit

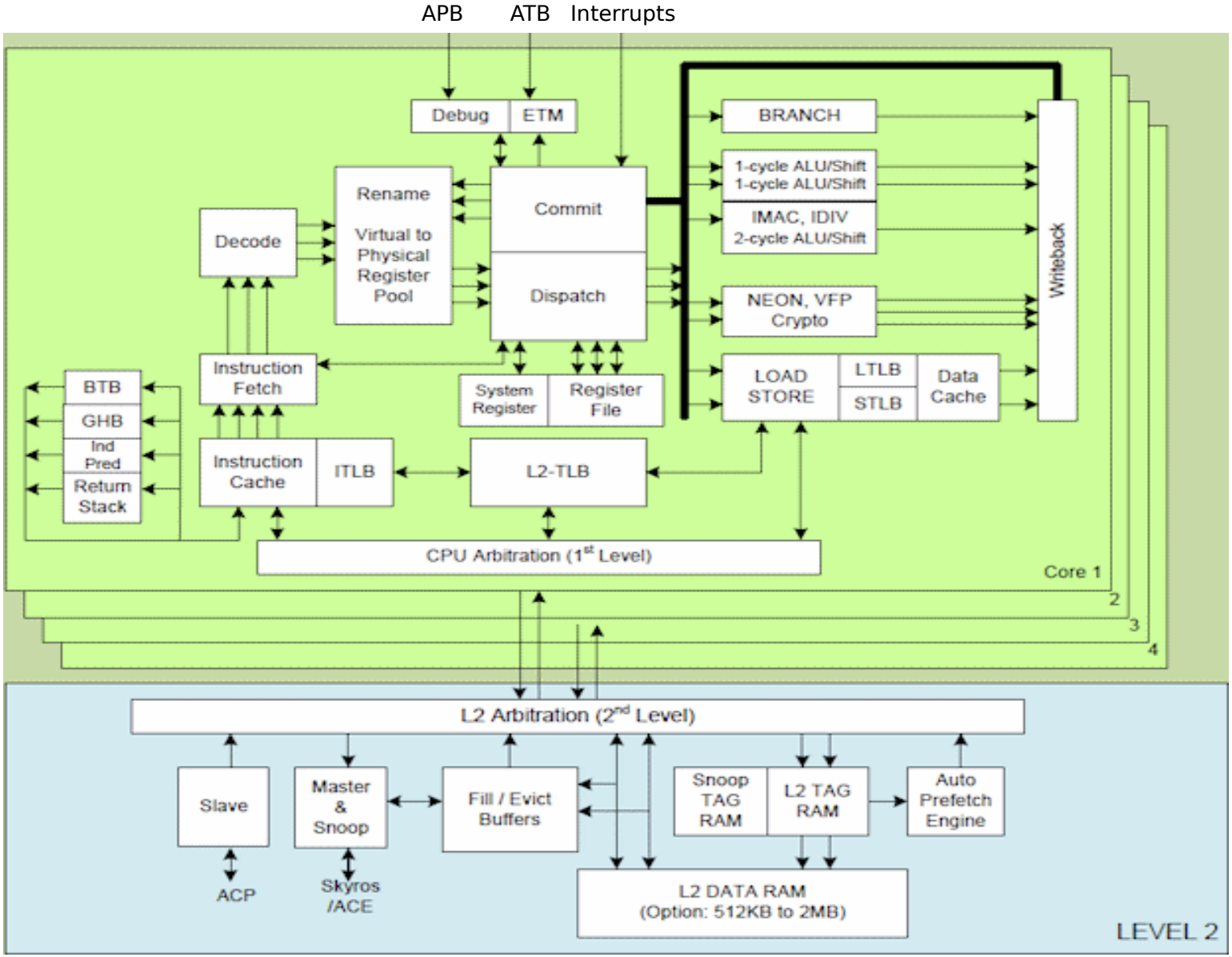
AMBA: Advanced Microcontroller Bus Architecture
(On-chip bus standard for SoC) designs)

ACE: AXI Coherency Extensions
(Used in big.LITTLE systems for smartphones, tablets, etc.)

AXI: Advanced eXtensible Interface
(The most widespread AMBA interface).

7.2 The 64-bit high performance Cortex-A57 (5)

Main functional blocks of the 64-bit high performance Cortex-A57 CPU [74]



7.2 The 64-bit high performance Cortex-A57 (6)

Remarks: Non trivial abbreviations in the above Figure

ATB: AMBA Trace Bus

APB: Advanced Peripheral Bus

ACP: Accelerator Coherence Port
(to connect non-cached coherent data sources)

ACE: AXI Coherency Extensions
(Used in big.LITTLE systems for smartphones, tablets, etc.)

AXI: Advanced eXtensible Interface
(The most widespread AMBA interface).

7.2 The 64-bit high performance Cortex-A57 (7)

Key features of the microarchitecture of the Cortex-A57 core -1

- Each core fetches four instructions per cycle from the Icache,
- decodes and renames three microinstructions per cycle,
- dispatches three microinstructions per cycle to the issue queues,
- whereas the issue queues issue up to eight microinstructions per cycle to the eight available execution units.

There are eight execution units available, as follows:

- a branch unit
- dual single cycle integer units
- a multi-cycle integer MAC/DIV/CRC unit
- dual Advanced SIMD (NEON)/FP. Crypto units and
- dual load/store units.

7.2 The 64-bit high performance Cortex-A57 (8)

Key features of the microarchitecture of the Cortex-A57 core -2

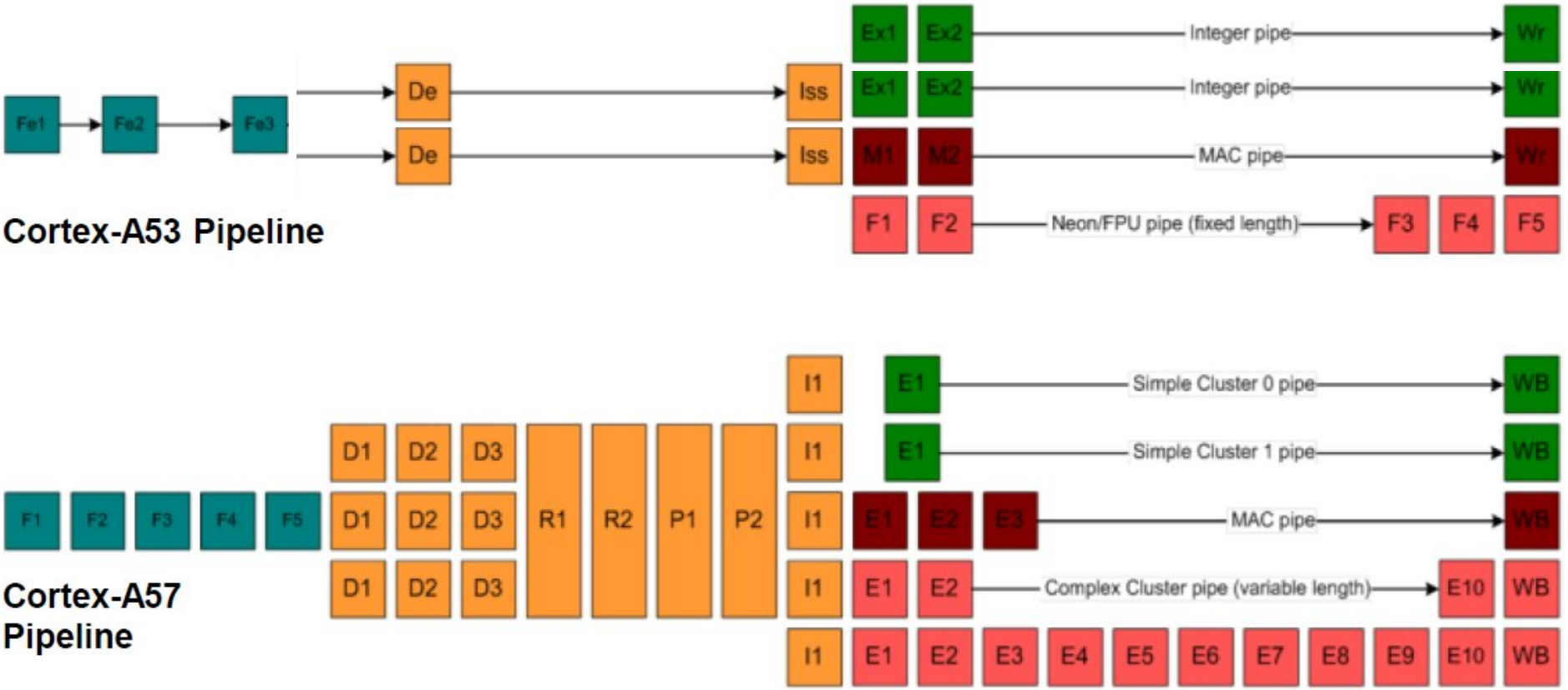
- Core efficiency: 4.8 DMIPS/MHz
- Expected core frequency up to 2.5 GHz in a 16 nm process implementation.

7.2 The 64-bit high performance Cortex-A57 (9)

Pipeline of the Cortex-A57 core -1

- The Cortex-A57 core has a 15 stages long integer pipeline with additional pipeline stages for NEON and FP processing, as indicated in the next two Figures.

Contrasting the Cortex-A53 and Cortex-A57 arithmetic pipelines [Based on 54]



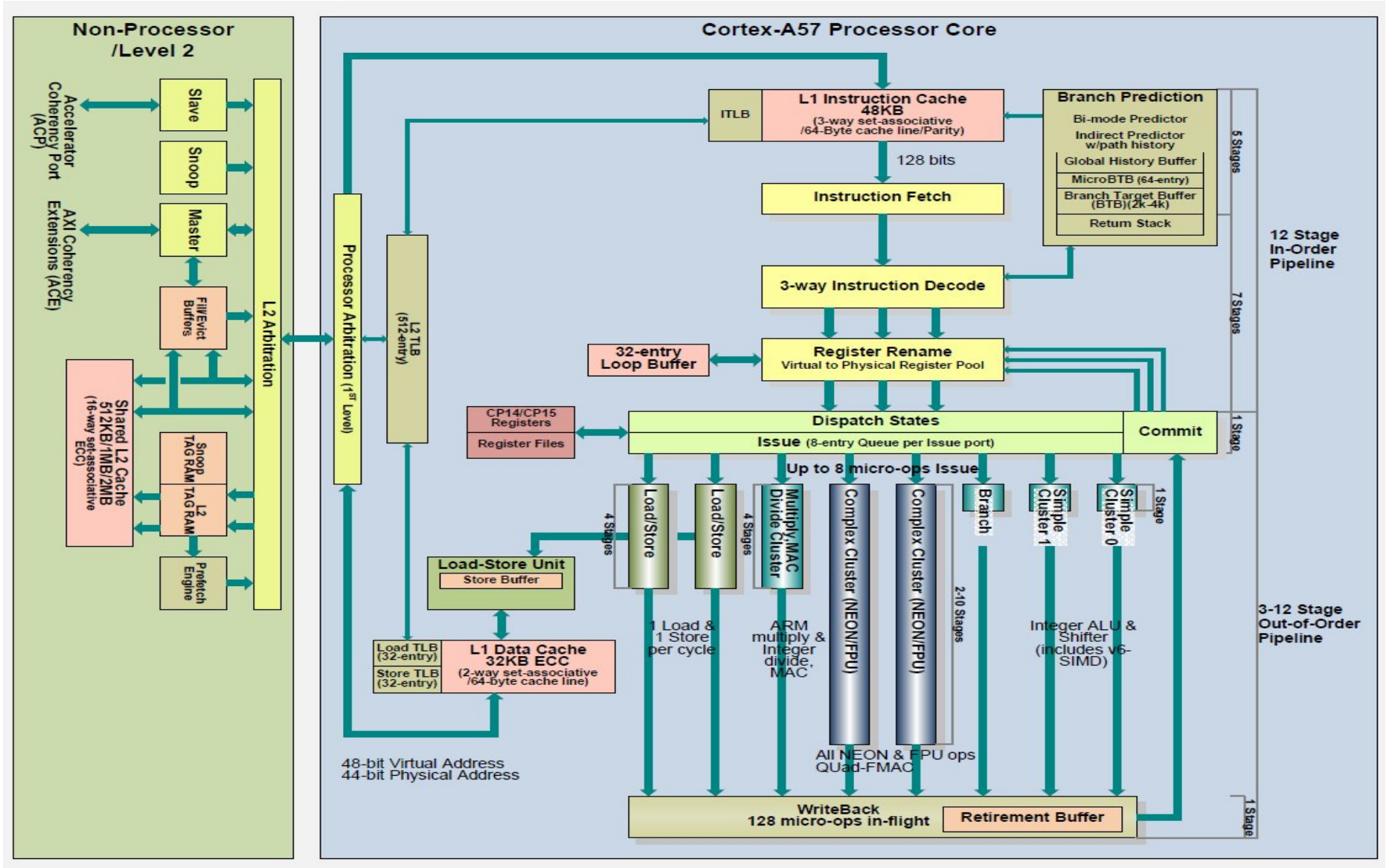
D: Decode
R: Rename
P: Dispatch
I: Issue
E: Execute
WB: Write Back

Note: Branch and Load/Store pipelines not shown

(1x Load/Store pipeline for the Cortex A-53 and
2x Load/Store and 1x Branch pipeline for the Cortex-A-57)

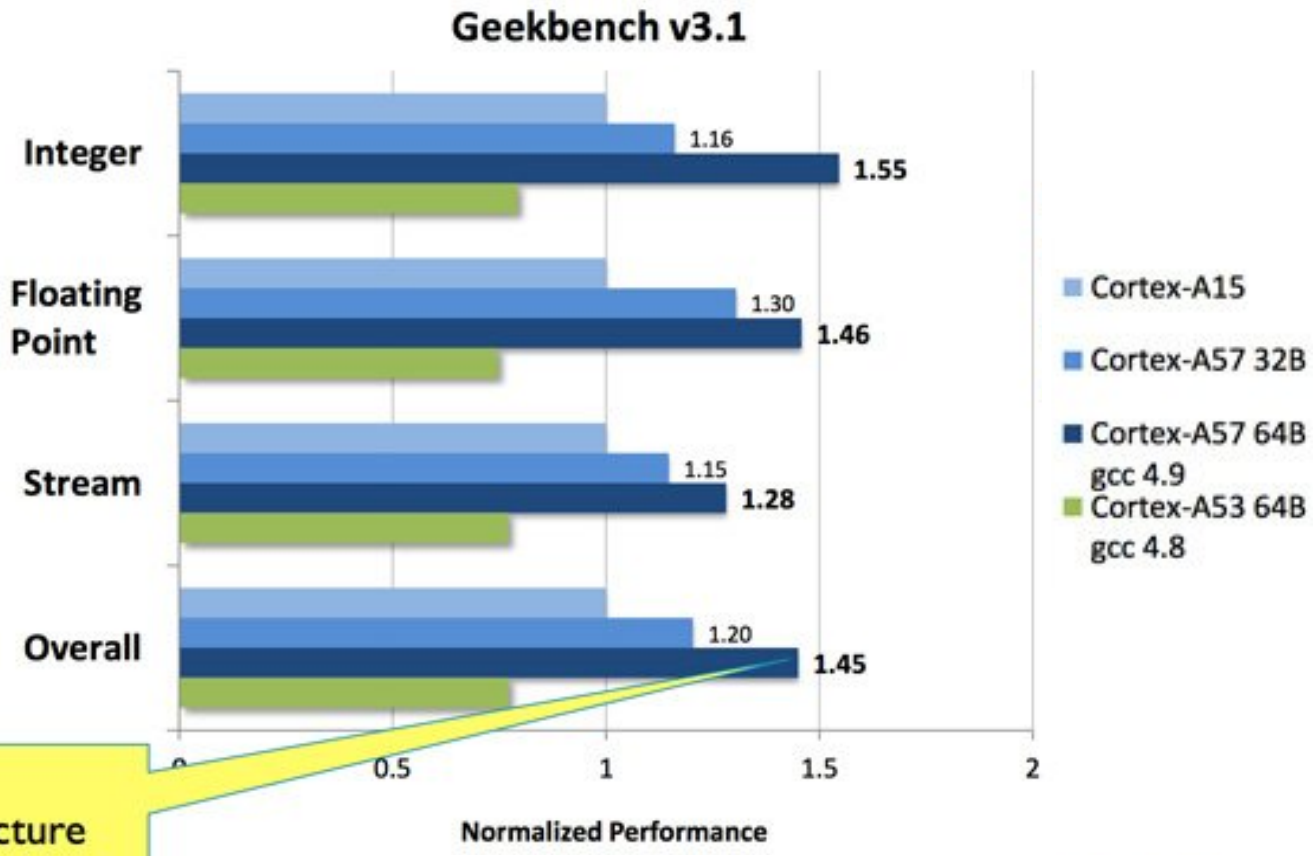
7.2 The 64-bit high performance Cortex-A57 (11)

Pipeline structure of the Cortex-A57 core (alternative view) [71]



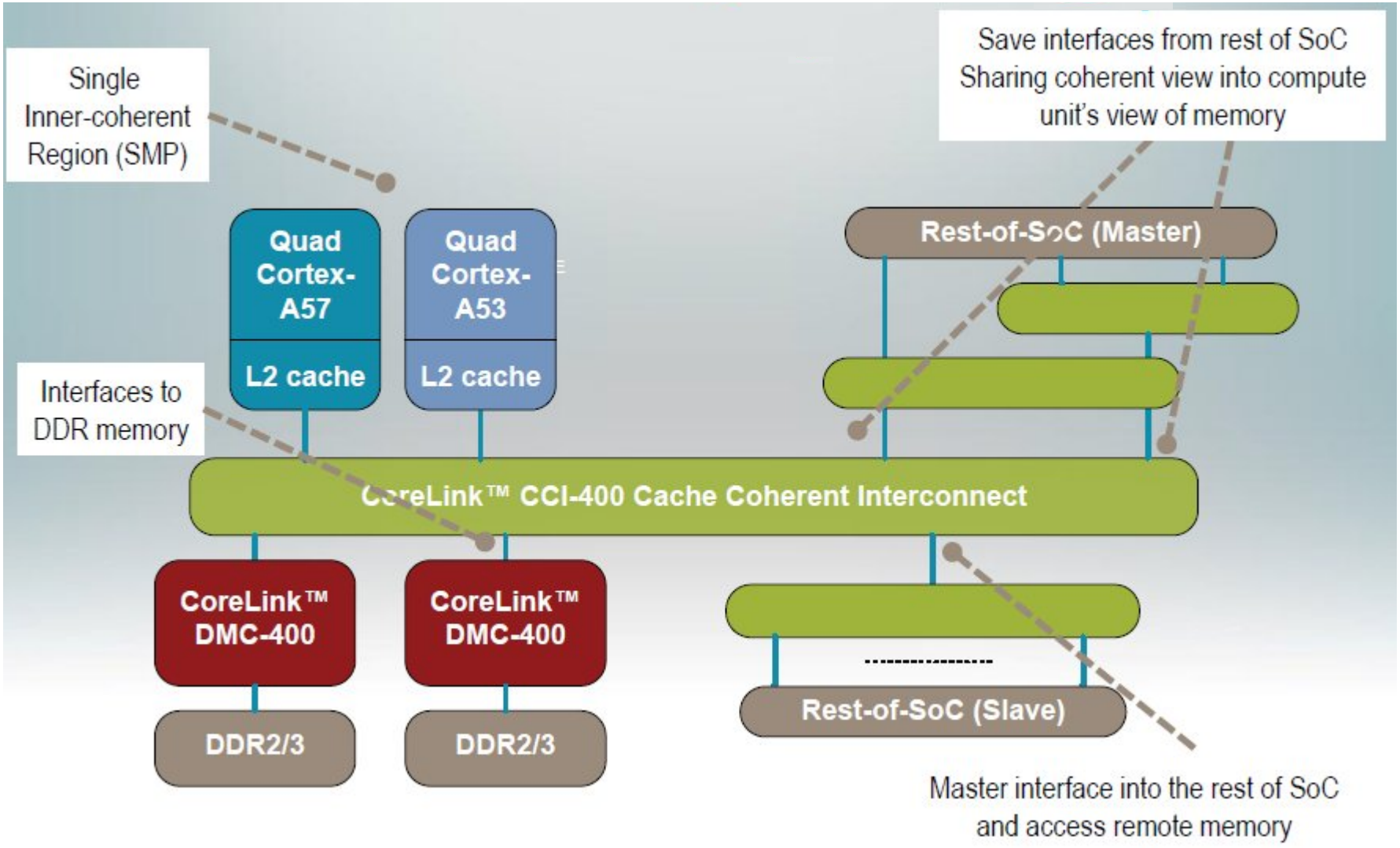
7.2 The 64-bit high performance Cortex-A57 (12)

Cortex-A57/A53 performance - compared to the Cortex-A15 [55]



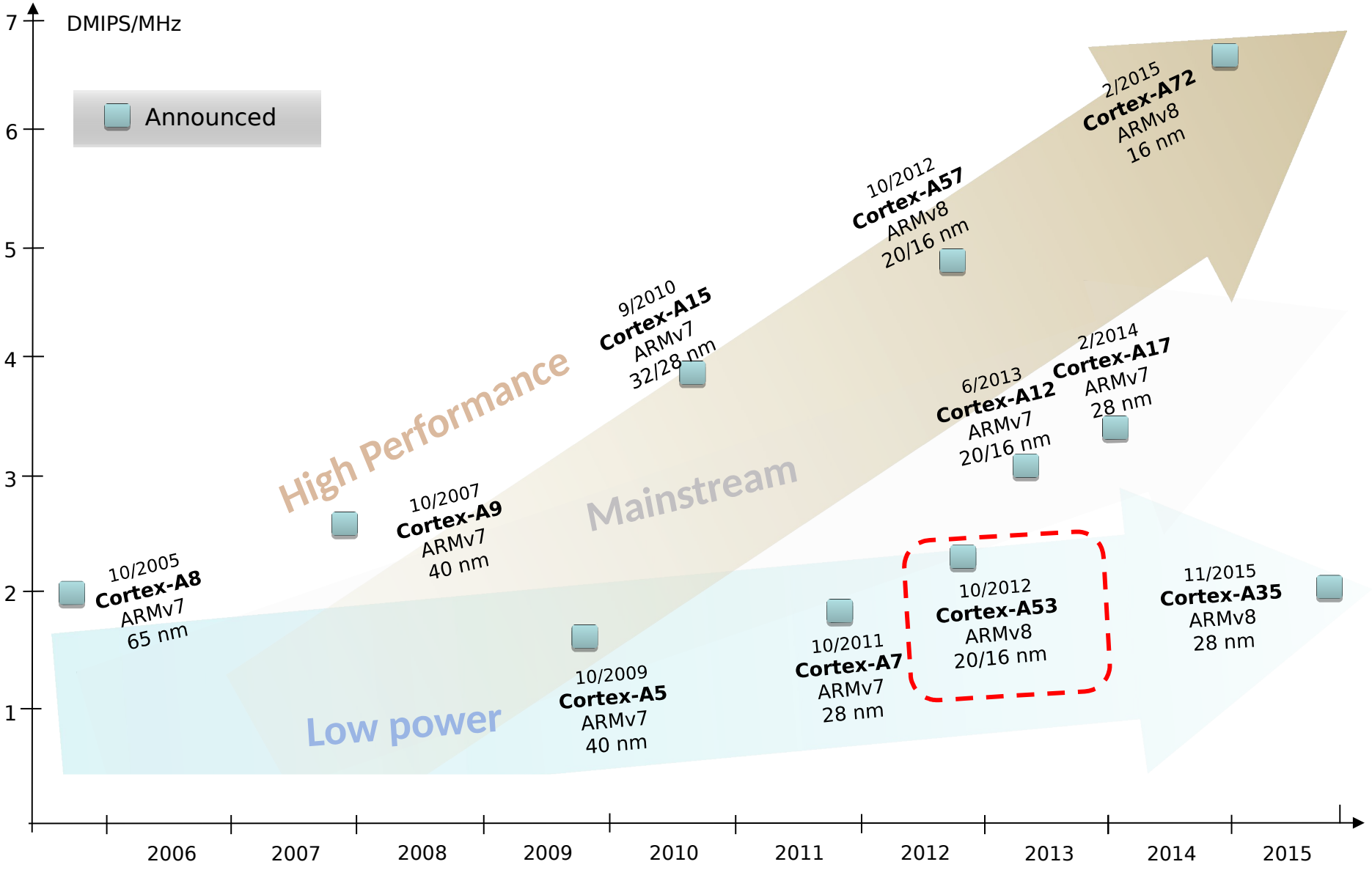
7.2 The 64-bit high performance Cortex-A57 (13)

Example: A Cortex-A57/Cortex-A53 big.LITTLE system [52]



7.3 The 64-bit low power Cortex-A53

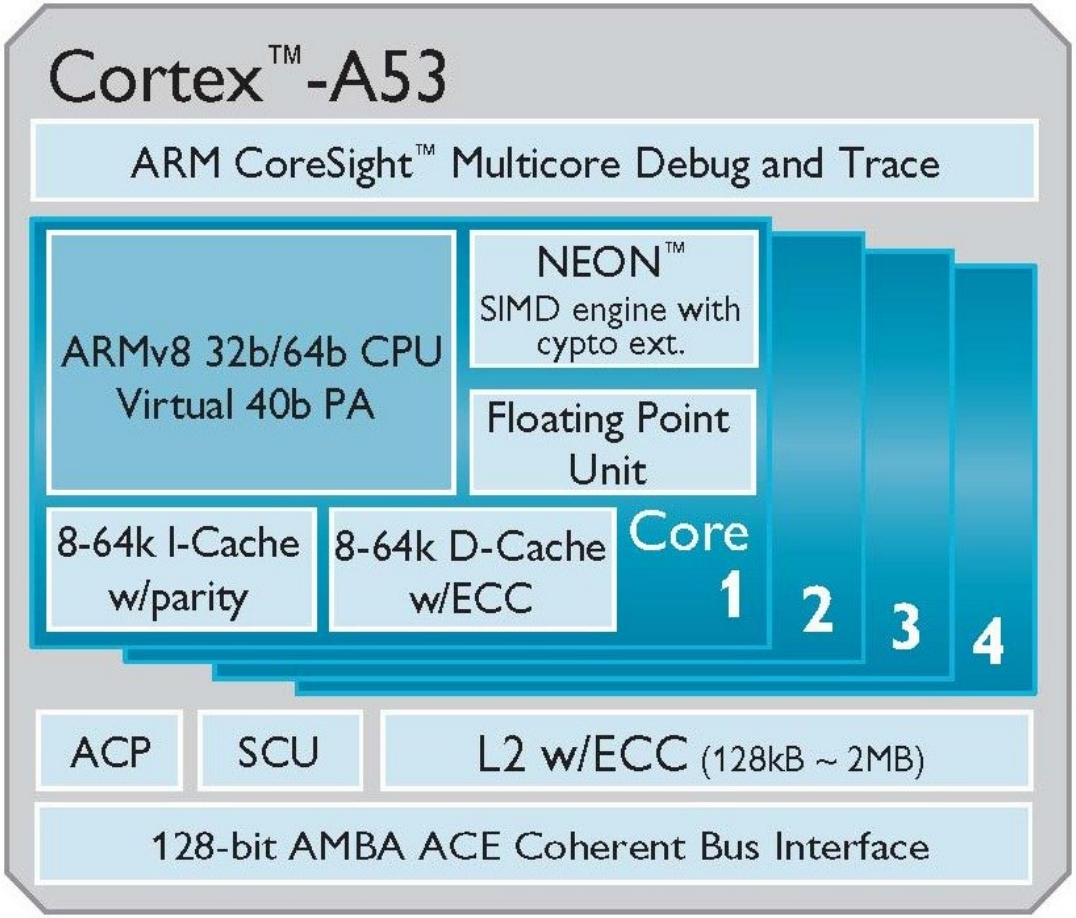
7.3 The 64-bit low power Cortex-A53 -1 (based on [12])



The 64-bit low power Cortex-A53 -2 [12]

- 10/2012: Announced along with the performance oriented Cortex-A57 processor, with immediate availability for licensing.
- 2014: First mobile devices with the Cortex-A53.
- It is the 64-bit successor to the Cortex-A7.
- The A57 and A53 models can be used either as stand alone processors or as components in a big-LITTLE configuration, similar to the 32-bit Cortex-A15 and A7 models.
- Target process technology: 16 or 20 nm.

High level block diagram of the Cortex-A53 [53]



PA: Physical Address

DED: Double Error Detection

ECC: Error Correcting Code

ACP: Accelerator Coherence Port
(to connect non-cached coherent data sources)

SCU: Snoop Control Unit

AMBA: Advanced Microcontroller Bus Architecture
(On-chip bus standard for SoC) designs)

ACE: AXI Coherency Extensions
(Used in big.LITTLE systems for smartphones, tablets, etc.)

AXI: Advanced eXtensible Interface
(The most widespread AMBA interface).

7.3 The 64-bit low power Cortex-A53 (4)

Key features of the microarchitecture of the Cortex-A53 core -1

- Fully compatible with the preceding ARMv7 32-bit ISA.
- Integrated L2 cache of 128 kB to 2 MB.
- Up to 4 Cortex-A53 CPU cores that execute the ARMv8 64-bit ISA.
- 128-bit AMBA coherent interface for connecting multiple (up to 4) Cortex-A53 processors.
- System wide cache coherence supported by a Snoop Control Unit (SCU).

Remarks

AMBA: Advanced Microcontroller Bus Architecture
(On-chip bus standard for SoC) designs

7.3 The 64-bit low power Cortex-A53 (5)

Key features of the microarchitecture of the Cortex-A53 core -2

- The Cortex-A53 core has a dual-issue in-order front end with 5 pipelines constituting the back end, as indicated in the next Figure.

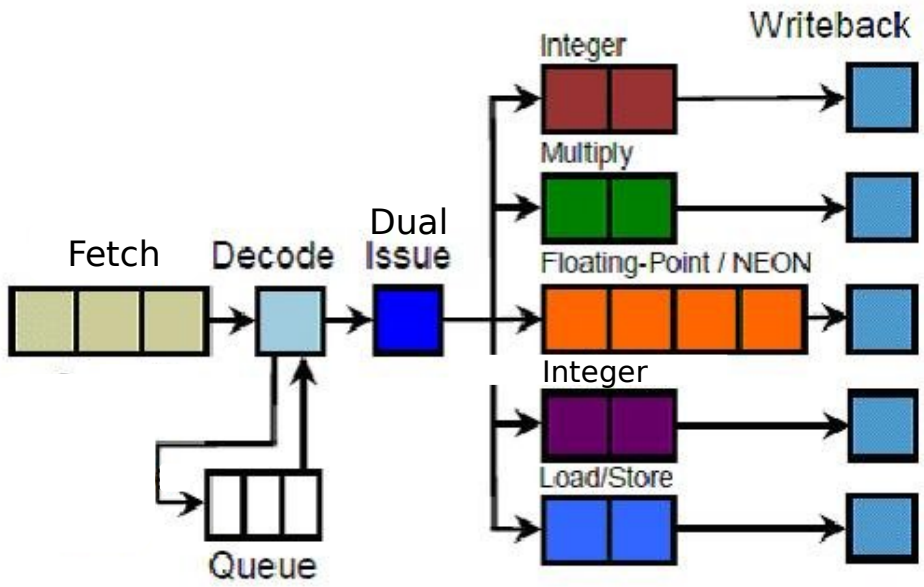


Figure: Pipeline stages of the Cortex-A53 [76]

- The pipeline for integer processing has 8 pipeline stages, NEON and FP processing has two additional pipeline stages, as seen in the Figure above.

7.3 The 64-bit low power Cortex-A53 (6)

Contrasting the Cortex-A7 and Cortex-A53 microarchitectures [75]

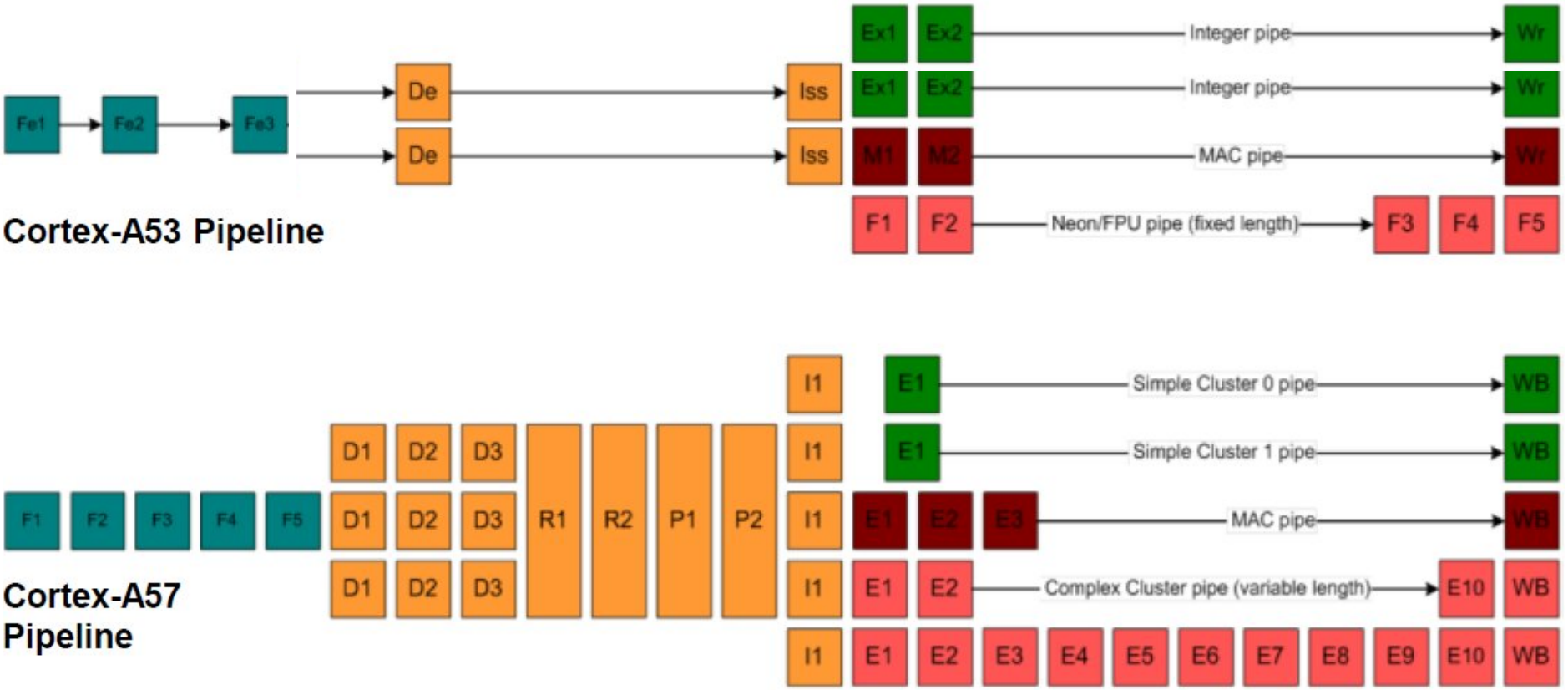
ARM CPU Core Comparison		
	Cortex-A7	Cortex-A53
ARM ISA	ARMv7 (32-bit)	ARMv8 (32/64-bit)
Issue Width	Partially 2 micro-ops	2 micro-ops
Pipeline Length	8	8
Integer Add	2	2
Integer Mul	1	1
Load/Store Units	1	1
Branch Units	1	1
FP/NEON ALUs	1x64-bit	1x64-bit
L1 Cache	8KB-64KB I$ + 8KB-64KB D$	8KB-64KB I$ + 8KB-64KB D$
L2 Cache	128KB - 1MB (Optional)	128KB - 2MB (Optional)

7.3 The 64-bit low power Cortex-A53 (7)

Remarks [75]

- We note that the Cortex-A7 has a partially dual-issue capability, meaning that the second issue slot can only issue branch and integer operations.
- In the Cortex-A53 the second issue slot can also issue load-store and FP/NEON operations.
- In additon, the branch prediction capabilities of the A53 were also significantly improved by including conditional and indirect jump predictors.

Contrasting the Cortex-A53 and Cortex-A57 arithmetic pipelines [Based on 54]



D: Decode
R: Rename
P: Dispatch
I: Issue
E: Execute
WB: Write Back

Note: Branch and Load/Store pipelines not shown

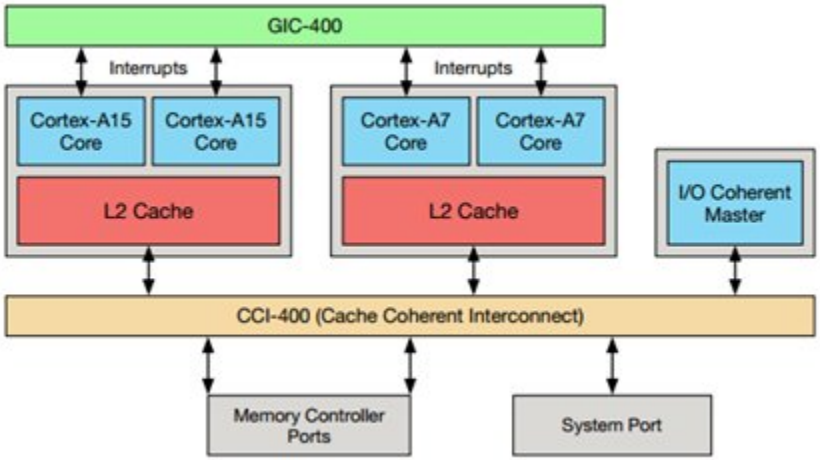
(1x Load/Store pipeline for the Cortex A-53 and
2x Load/Store and 1x Branch pipeline for the Cortex-A-57)

7.3 The 64-bit low power Cortex-A53 (9)

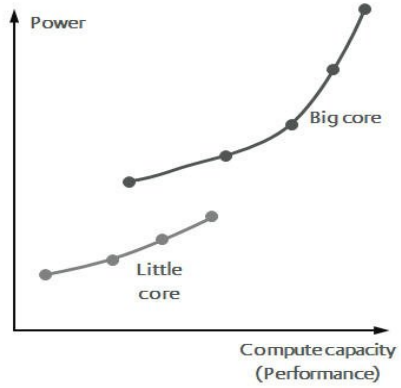
Key features of the microarchitecture of the Cortex-A53 core -3

- Core efficiency: 2.3 DMIPS/MHz
- Expected core frequency up to 1.5 GHz.

Architettura big.LITTLE



- Cluster di core ARM Cortex-A15
- Cluster di core ARM Cortex-A7
- Cache condivisa di secondo livello
- Cache Coherent Interconnect (CCI)
- Coherent Master I/O
- Generic Interrupt Controller (GIC)

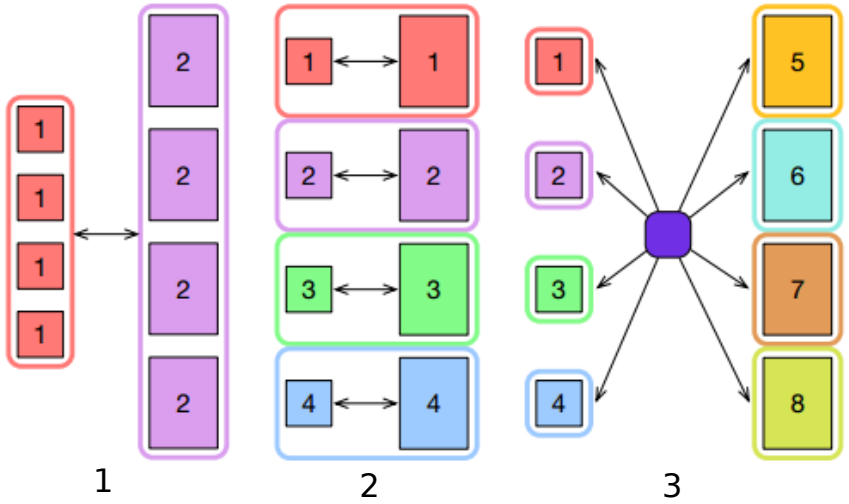


I cluster hanno consumi differenti a seconda delle prestazioni

Quindi è necessaria una scelta opportuna del cluster da utilizzare

Architettura big.LITTLE

Politiche di Scheduling



1. Migrazione cluster
2. Migrazione CPU
3. Global Task Scheduling

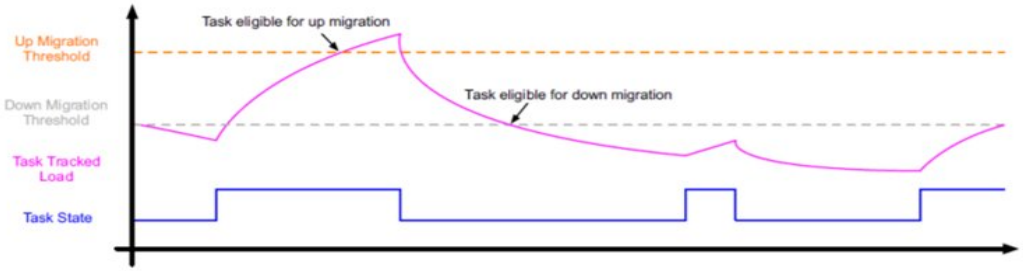
1. Migrazione cluster: vengono raggruppati in base al tipo big o LITTLE con lo scheduler che attiva uno dei due, lasciando spento l’altro

2. Migrazione CPU: stesso numero di core in big e LITTLE, con accoppiamento 1:1. In ogni coppia, c'è un solo nucleo attivo alla volta, mentre l'altro è spento

3. GTS: Lo scheduler analizza le prestazioni richieste da ciascun

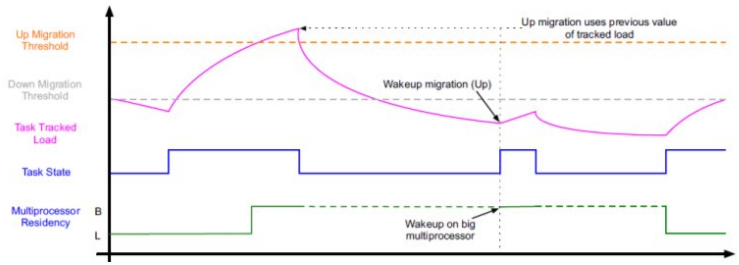
Architettura big.LITTLE

Metrica

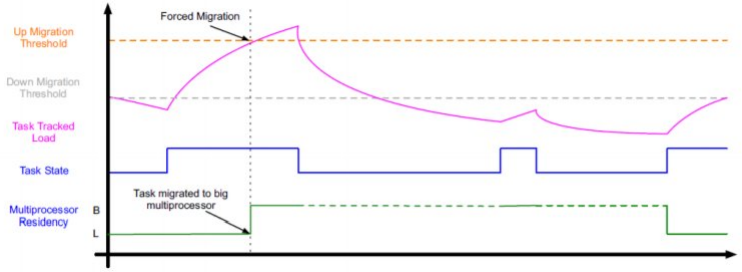


Tracciato di carico di un task: elemento di valutazione dell'allocazione del task verso i cluster attraverso le soglie Up e Down che ne vanno a definire la metrica.

Se il tracciato di carico del task eccede la soglia superiore o



Awake Migration



Forced Migration

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