# William Stallings
# Computer Organization and Architecture
# 7th Edition

## Chapter 3

## System Buses

# Agenda

- Concetti generali
  - Revisione dell'architettura dei calcolatori
  - Comunicazione tra componenti - Interruzioni
- I BUS
  - Principi Fondamentali – Tipi di Bus e Topologie
  - Caratteristiche dei BUS
- PCI
  - Caratteristiche di PCI
  - Operazioni di READ/Write
  - Arbitraggio

# Concetti Generali ( ... un po' di ripasso ...)

# Program Concept

- Hardwired systems are inflexible
- General purpose hardware can do different tasks, given correct control signals
- Instead of re-wiring, supply a new set of control signals

# What is a program?

- A sequence of steps
- For each step, an arithmetic or logical operation is done
- For each operation, a different set of control signals is needed

# Function of Control Unit

- For each operation a unique code is provided
  - e.g. ADD, MOVE
- A hardware segment accepts the code and issues the control signals

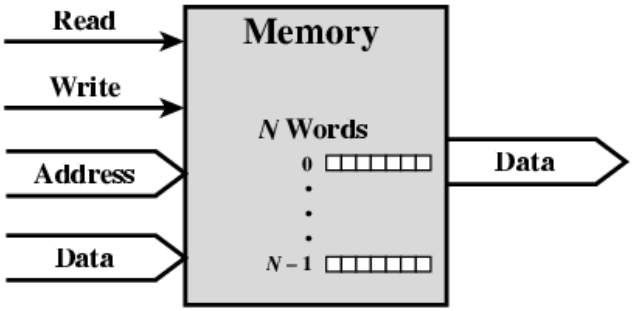
- We have a computer!

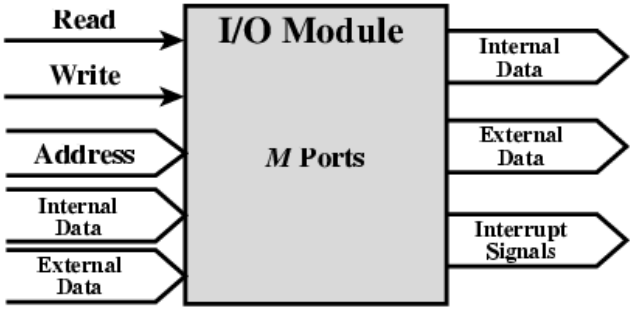
# Interconnessioni tra Componenti

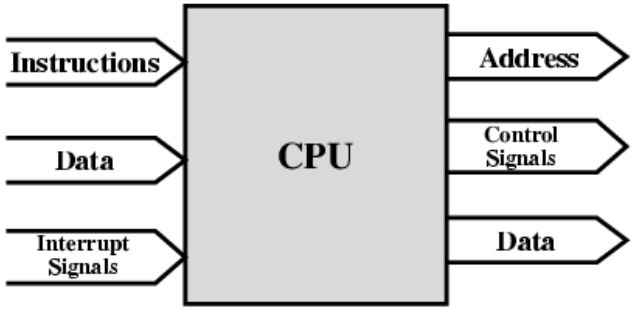
# Connecting

- All the units must be connected
- Different type of connection for different type of unit
  - Memory
  - Input/Output
  - CPU

# Computer Modules



# Memory Connection

- Receives and sends data
- Receives addresses (of locations)
- Receives control signals
  - Read
  - Write
  - Timing

# Input/Output Connection(1)

- Similar to memory from computer's viewpoint
- Output
  - Receive data from computer
  - Send data to peripheral
- Input
  - Receive data from peripheral
  - Send data to computer

# Input/Output Connection(2)

- Receive control signals from computer
- Send control signals to peripherals
  - —e.g. spin disk
- Receive addresses from computer
  - —e.g. port number to identify peripheral
- Send interrupt signals (control)

# CPU Connection

- Reads instruction and data
- Writes out data (after processing)
- Sends control signals to other units
- Receives (& acts on) interrupts

# I BUS

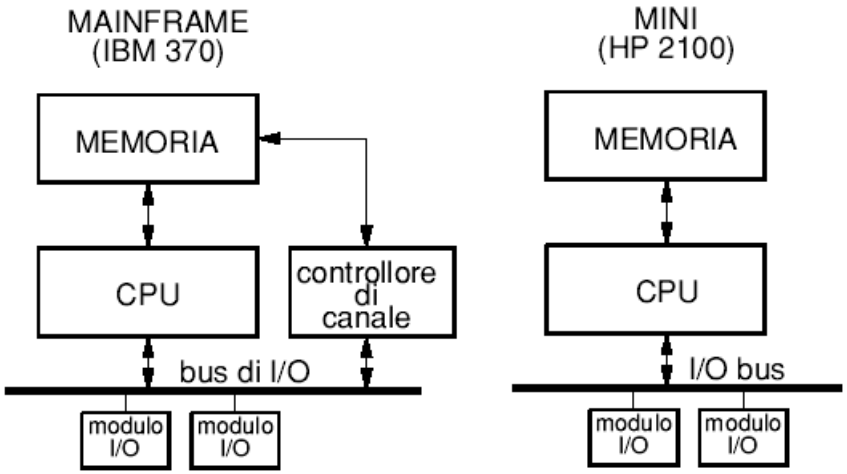
# Buses

- There are a number of possible interconnection systems
- Single and multiple BUS structures are most common
- e.g. Control/Address/Data bus (PC)
- e.g. Unibus (DEC-PDP)

# What is a Bus?

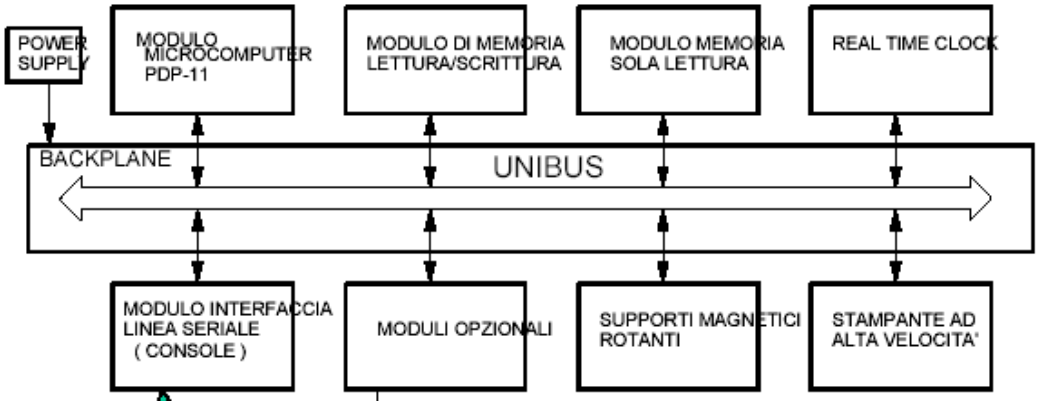
- A communication pathway connecting two or more devices
- Usually broadcast
- Often grouped
  - A number of channels in one bus
  - e.g. 32 bit data bus is 32 separate single bit channels
- Power lines may not be shown

# La nascita del Bus di Sistema: UNIBUS




Le Architetture dei primi sistemi IBM 370, HP 2100

L'UNIBUS



# Evoluzione dei BUS (I)

- IBM74 (Anni ’60)
  - Comunicazioni indipendenti
- UNIBUS (Anni ’60-’70)
  - Introduzione del Backplane, un unico canale
- BUS industriali e VME(dagli anni ’80)
  - Massimo utilizzo del concetto di bus di sistema, modularità portata all’estremo, lo standard VME

# Evoluzione dei BUS (II)

- I PC: dal PC Bus A PCI (dagli anni ’80 )
  - Molteplici Bus, sia per la compatibilità con il passato (ISA), che per la gestione dedicata di parti del sistema (AGP), il PCI come standard de facto
- Reti Industriali
  - I moduli diventano nodi di una rete, i concetti di bus di sistema e quello di rete si cominciano a confondere, lo standard Profibus

# Gli Standard

Esempi di noti standard

- IEEE 796 (Multibus I)
- IEEE 896 (Futurebus)
- IEEE 1014 (VME)
- IEC 61158 (Profibus, Foundation Fieldbus)

Devono definire

- Caratteristiche Meccaniche
- Caratteristiche Elettriche
- Caratteristiche Logico/Funzionali

# Sintesi di alcune Caratteristiche Meccaniche ed Elettriche

*Meccaniche*

- Inserzione
  - Diretta
  - Indiretta
- Dimensione
  - Standardizzazione delle Unità

*Elettriche*

- Logica Positiva o Negativa
- Tempi di ritardo
- Tempi di salita/discesa

# Caratteristiche Logico Funzionali

*Struttura*

- Dimensione del Bus
- Numero e tipo dei segnali
- Modalità
  - Sincrona
  - Asincrona
- Meccanismo di allocazione del Bus
- Gestione delle Interruzioni

*Protocollo*

- Insieme di regole per lo scambio dei segnali
- Descrizione della Tempificazione di ciascuno dei segnali coinvolti

# Tipi di BUS

- Data Bus
- Address Bus
- Control Bus

# Data Bus

- Carries data
  - Remember that there is no difference between "data" and "instruction" at this level
- Width is a key determinant of performance
  - 8, 16, 32, 64 bit

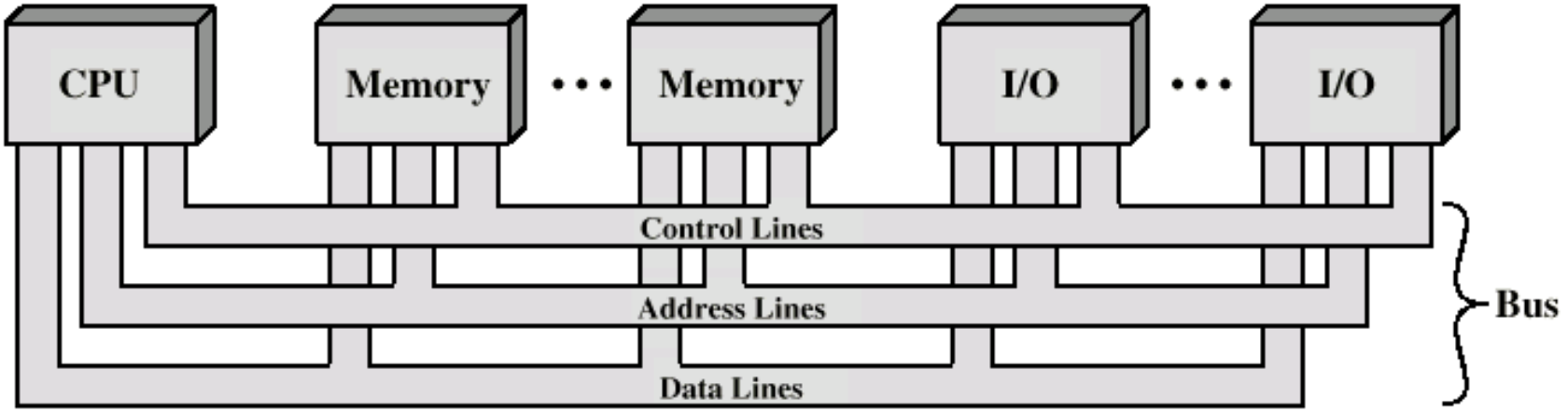
# Address bus

- Identify the source or destination of data
- e.g. CPU needs to read an instruction (data) from a given location in memory
- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space

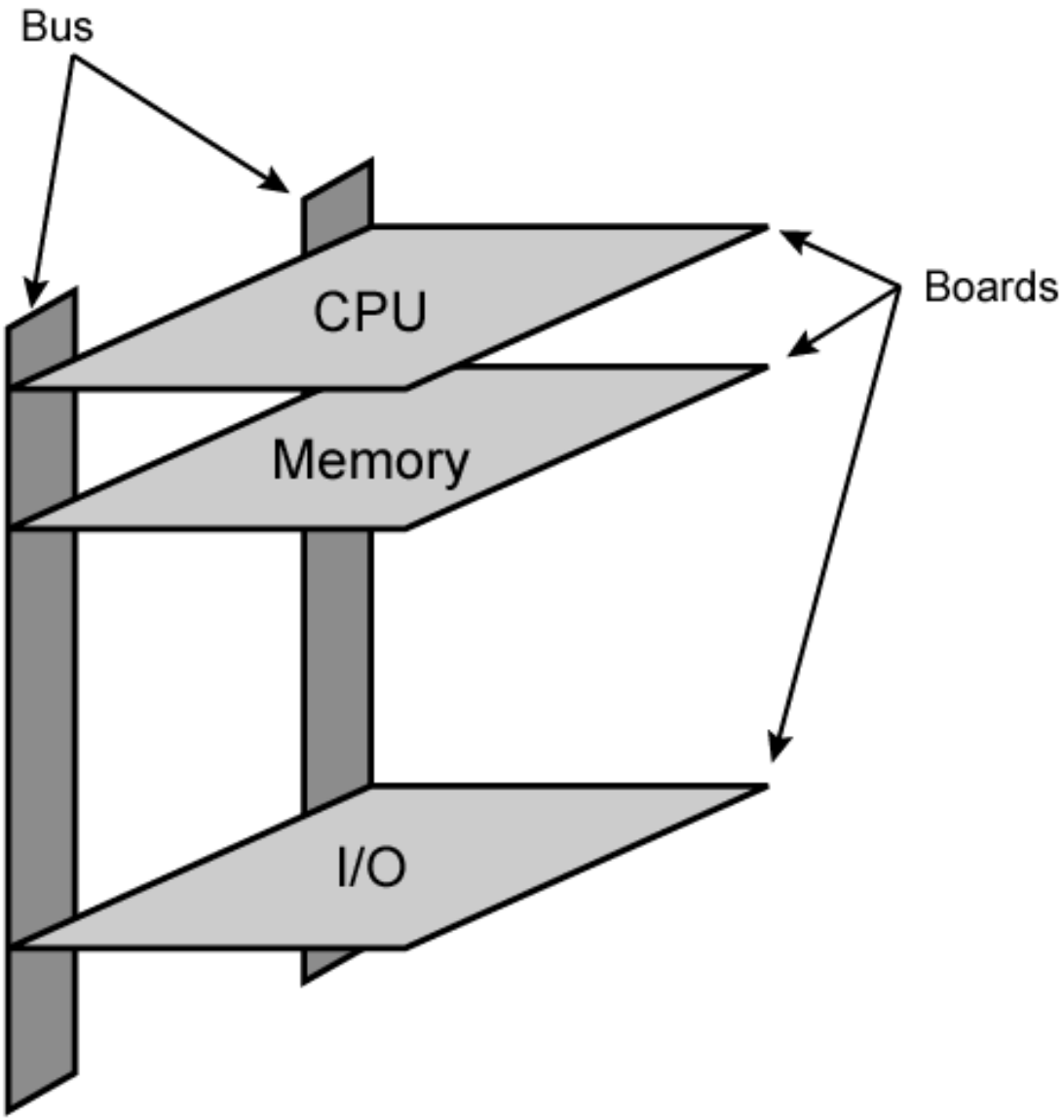
# Control Bus

- Control and timing information
  - Memory read/write signal
  - Interrupt request
  - Clock signals

# Bus Interconnection Scheme



# Physical Realization of Bus Architecture



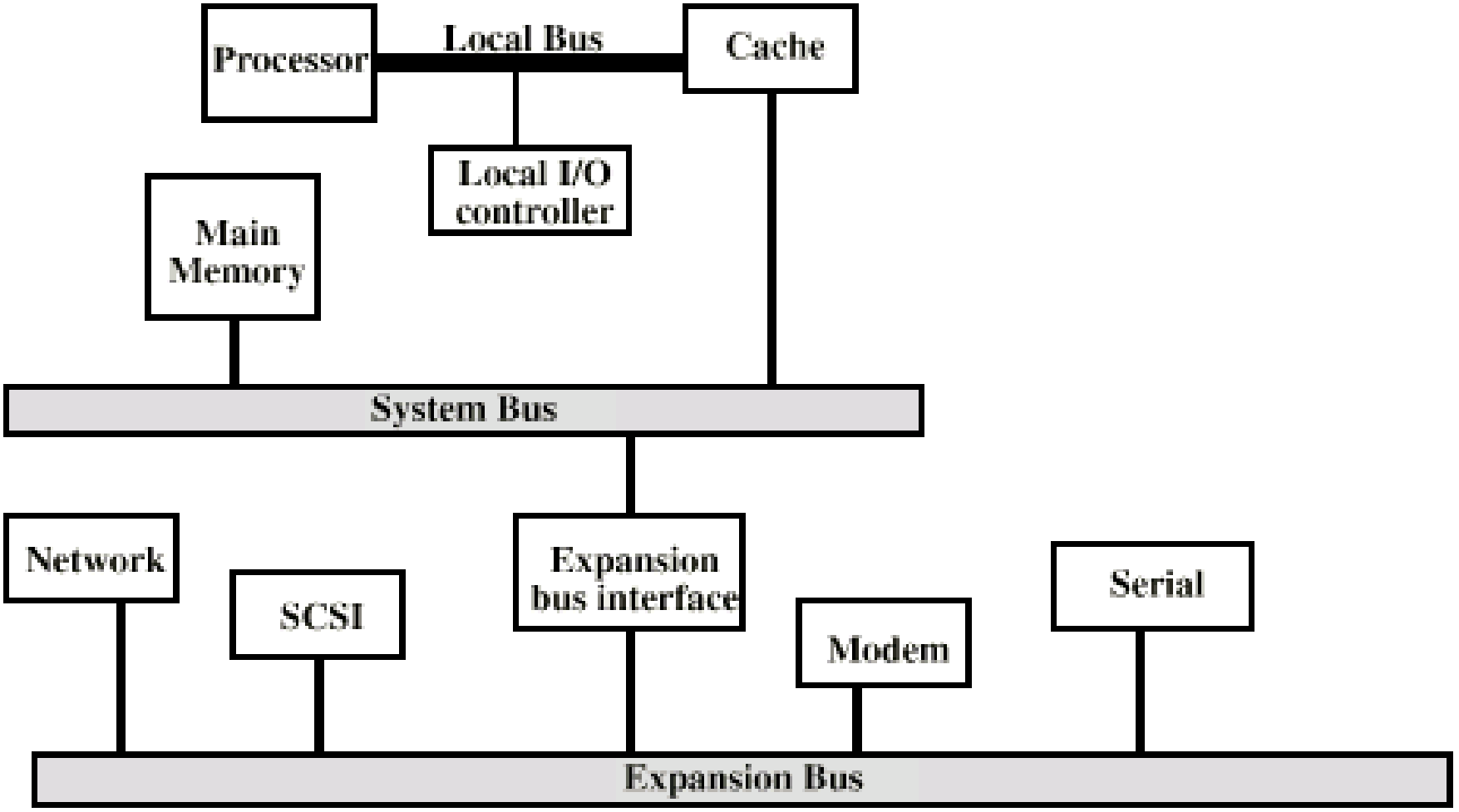
# Big and Yellow?

- What do buses look like?
  - Parallel lines on circuit boards
  - Ribbon cables
  - Strip connectors on mother boards
    - e.g. PCI
  - Sets of wires

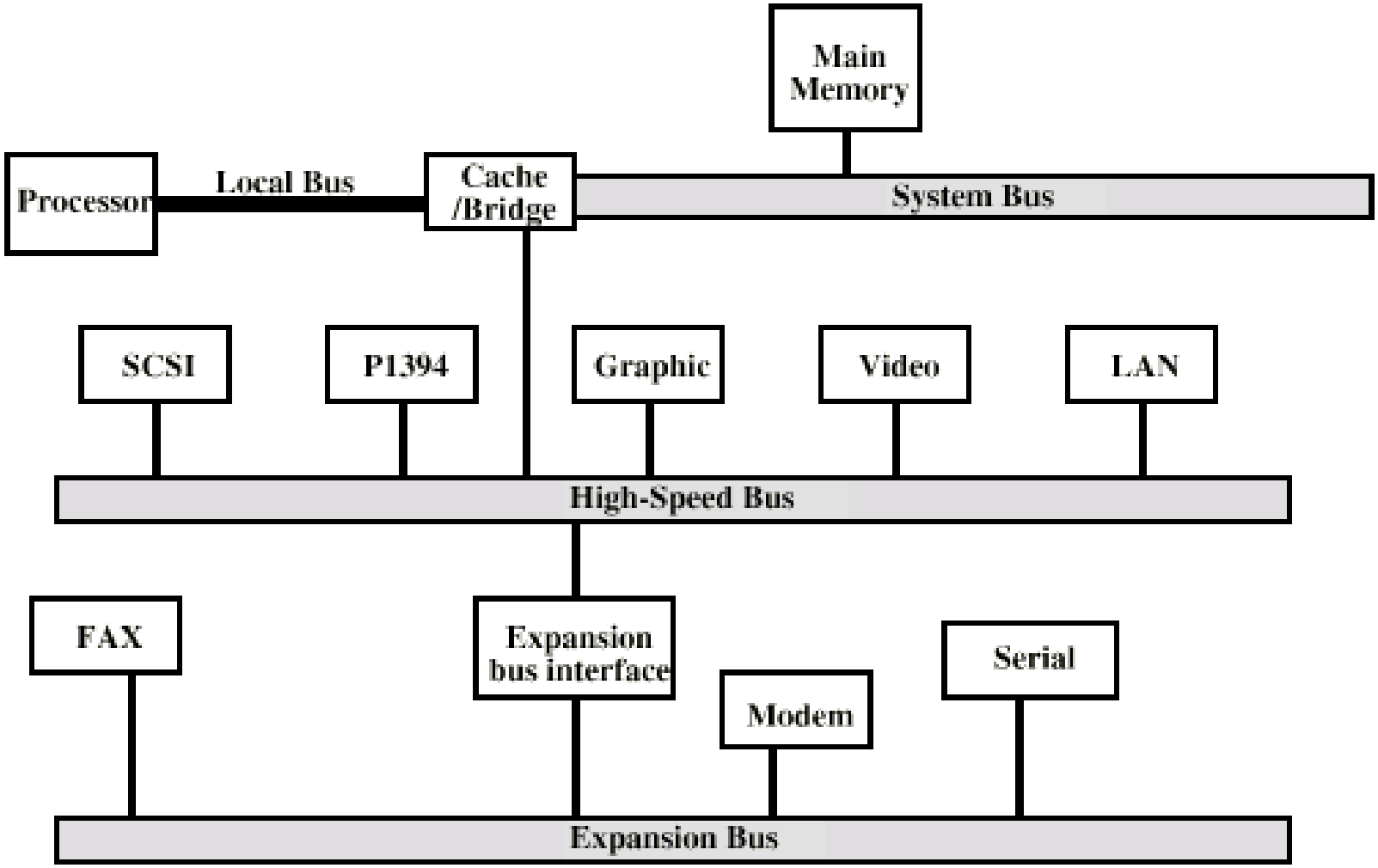
# Single Bus Problems

- Lots of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
    - If aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems

# Traditional (ISA) (with cache)



# High Performance Bus



# Bus Types

- Dedicated
  - Separate data & address lines
- Multiplexed
  - Shared lines
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Ultimate performance

# Bus Arbitration

- More than one module controlling the bus
- e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be centralised or distributed

# I ruoli dei Dispositivi

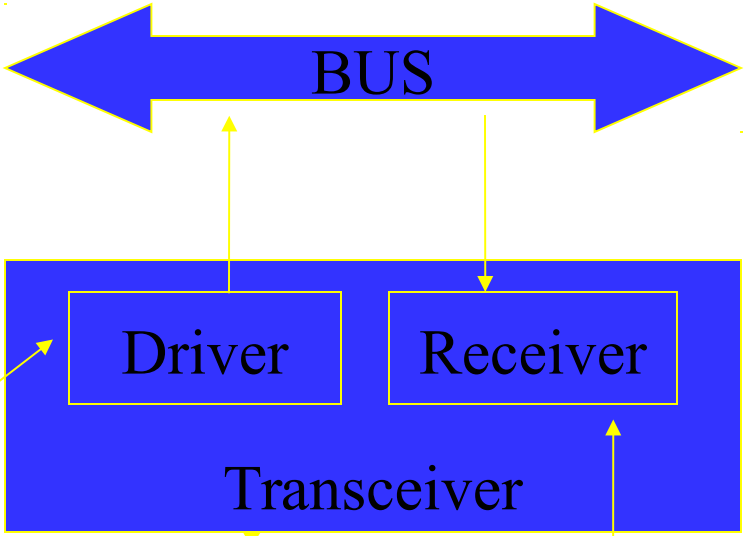
- Dispositivi Attivi (Master)
  - Sono in grado di avviare dei trasferimenti sul bus
- Dispositivi Passivi (Slave)
  - Sono in attesa, aspettando richieste di trasferimento

- Il ruolo di un dispositivo può cambiare nel tempo;
- un dispositivo può comportarsi da master o da slave in contesti differenti.
- Lo standard che definisce il bus deve fornire le regole per gestire tali condizioni o vietarle

# Cenni a Problemi Elettrici

## *- Driver del Bus -*

I segnali binari emessi dai dispositivi non sono in grado di alimentare il bus, il Driver del bus è esenzialmente un amplificatore digitale




Ruolo Master

Il Dispositivo è sia Master che Slave

Ruolo Slave

# Centralised or Distributed Arbitration

- Centralised
  - —Single hardware device controlling bus access
    - – Bus Controller
    - – Arbiter
  - —May be part of CPU or separate
- Distributed
  - —Each module may claim the bus
  - —Control logic on all modules

# Arbitraggio del Bus

*Il Problema*

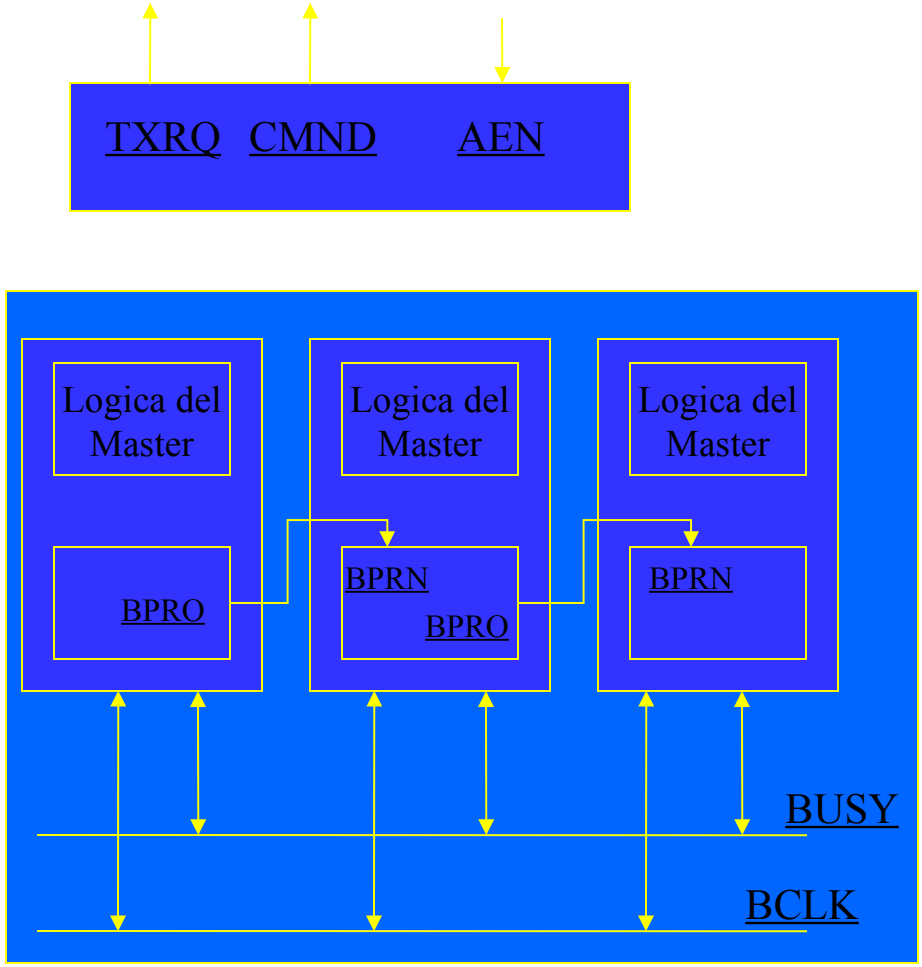
- Bus MultiMaster:
  - E’ ammesso più di un dispositivo Master sul BUS
- Arbitraggio:
  - Gestione delle contese tra i vari Master

*Le Soluzioni*

- Distribuito/ Daisy Chain
- Centralizzato/Parallelo
- Centralizzato/Daisy Chain

# Daisy Chain (Multibus I)

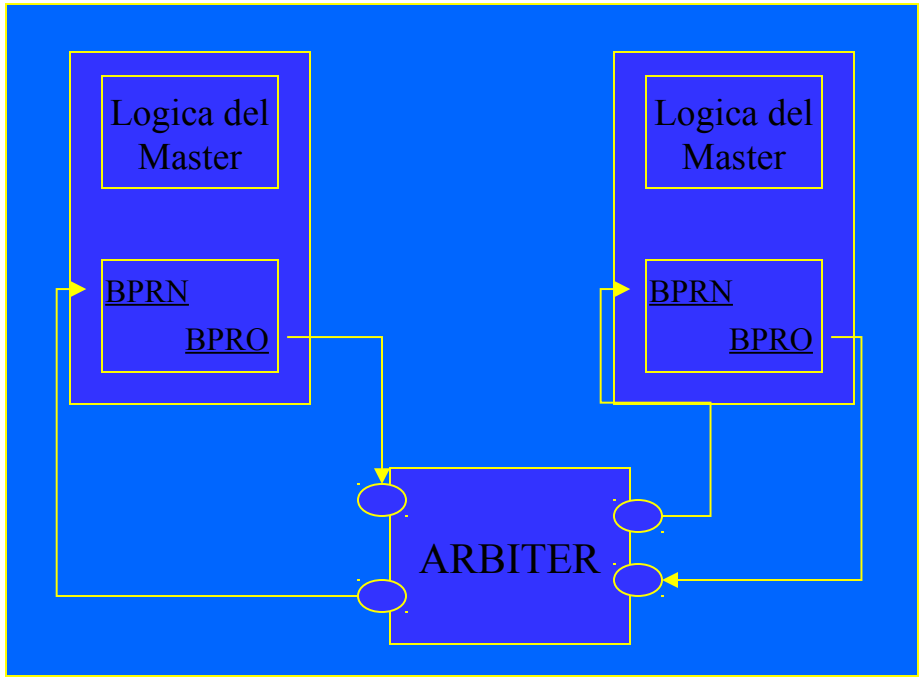
- Il Master che intende utilizzare la linea controlla la linea di BUSY
- Se libera la asserisce
- La Logica del Master richiede l'accesso al BUS



# Centralizzato Parallelo (Multibus I)

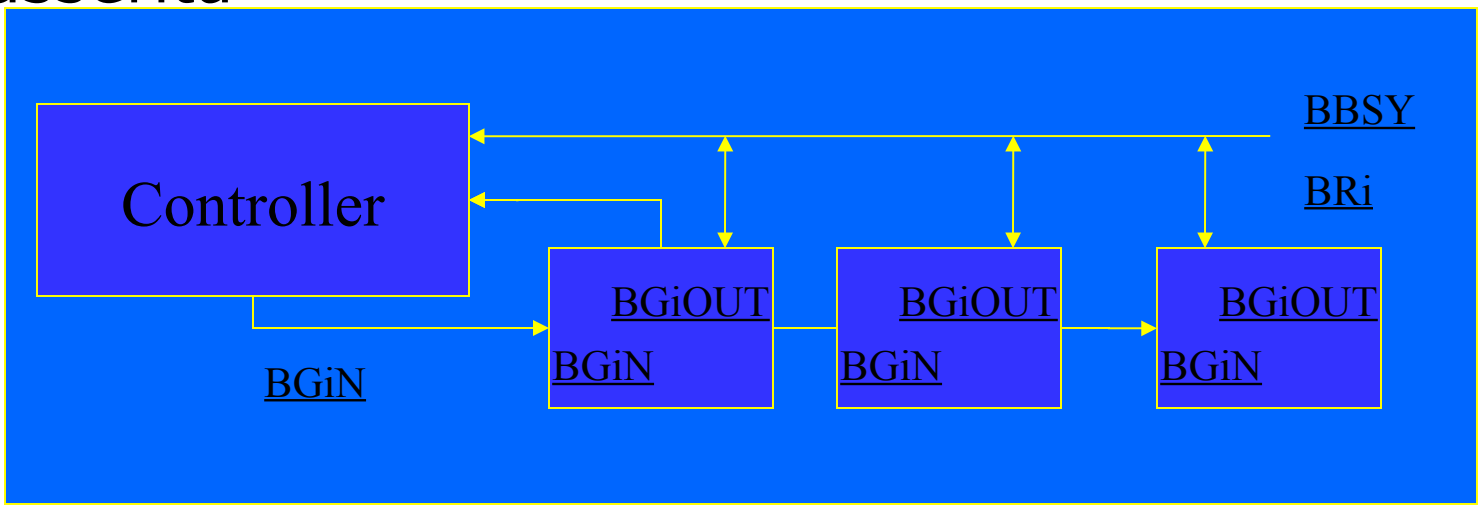
- Tutte le linee di richiesta vanno all'arbitro
- Tutte le linee di ack vanno all'arbitro
- L'arbitro definisce le priorità

*Nota: adottato anche in EISA e PCI*



# Centralizzato Daisy Chain (VME)

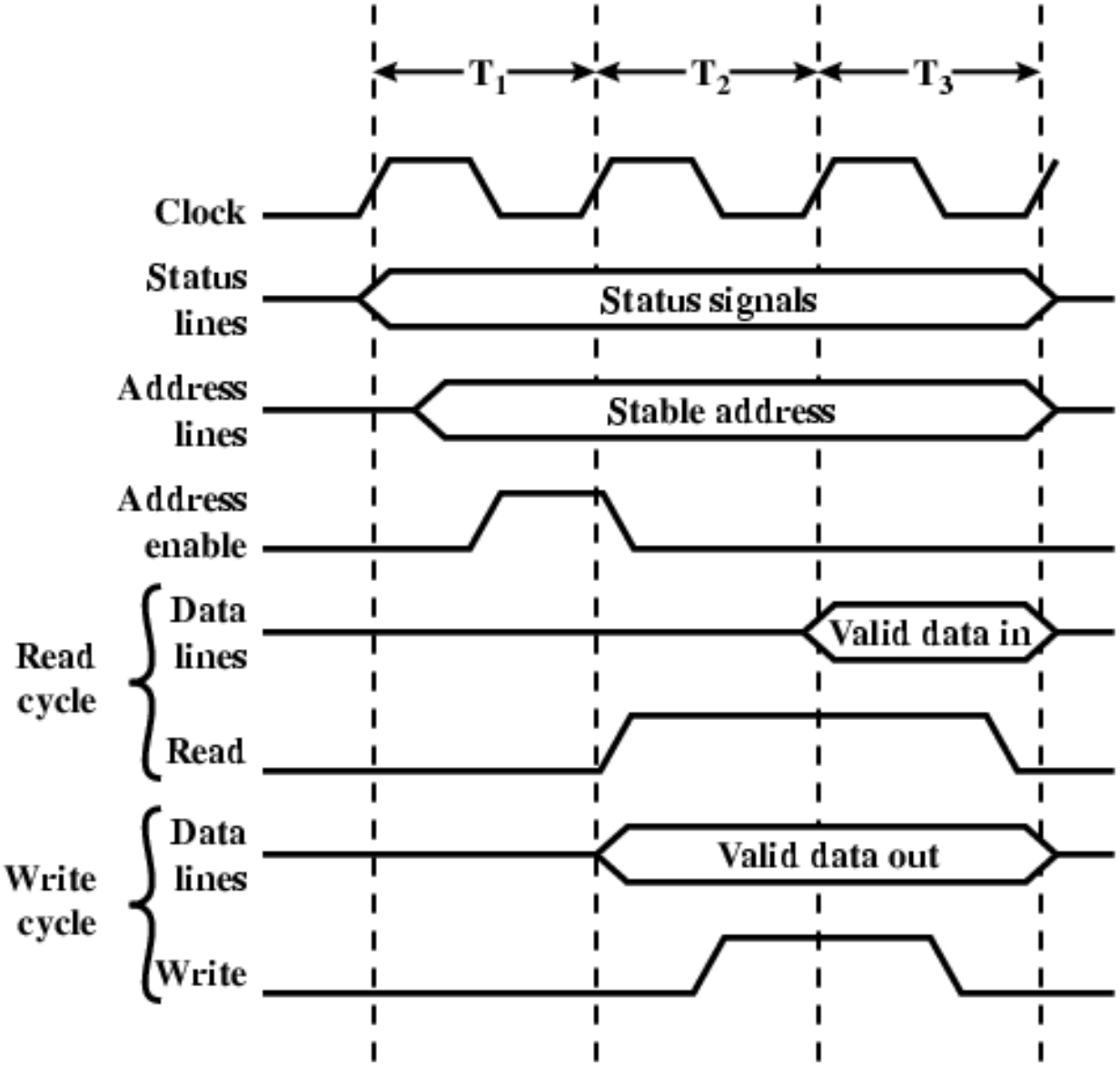
- Il Controllore gestisce diverse liste
- La Linea BBSY è comune a tutte e permette di sincronizzare le richieste
- Nessun modulo può fare richiesta con BBSY asserita



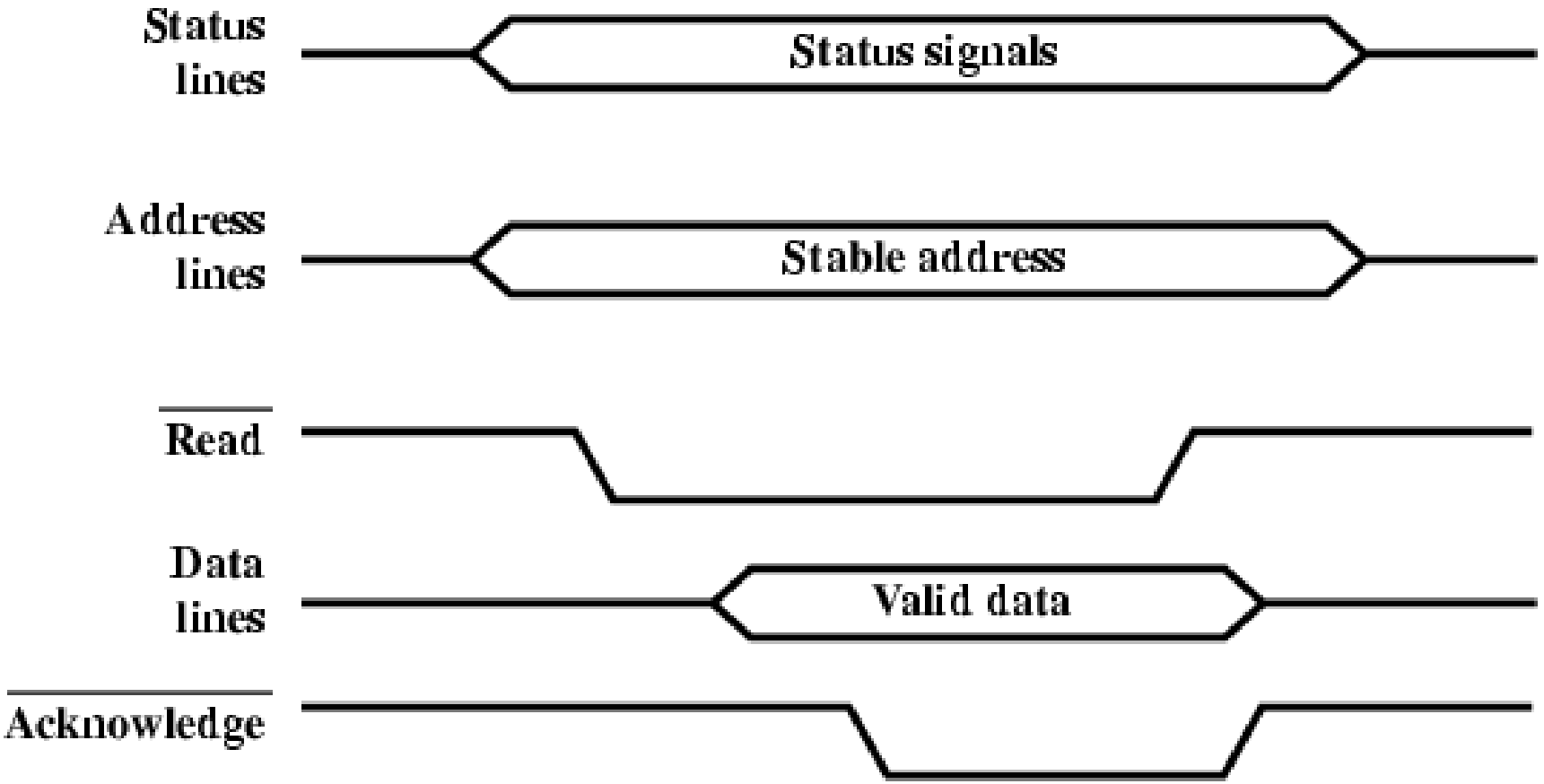
# Timing

- Co-ordination of events on bus
- Synchronous
  - Events determined by clock signals
  - Control Bus includes clock line
  - A single 1-0 is a bus cycle
  - All devices can read clock line
  - Usually sync on leading edge
  - Usually a single cycle for an event

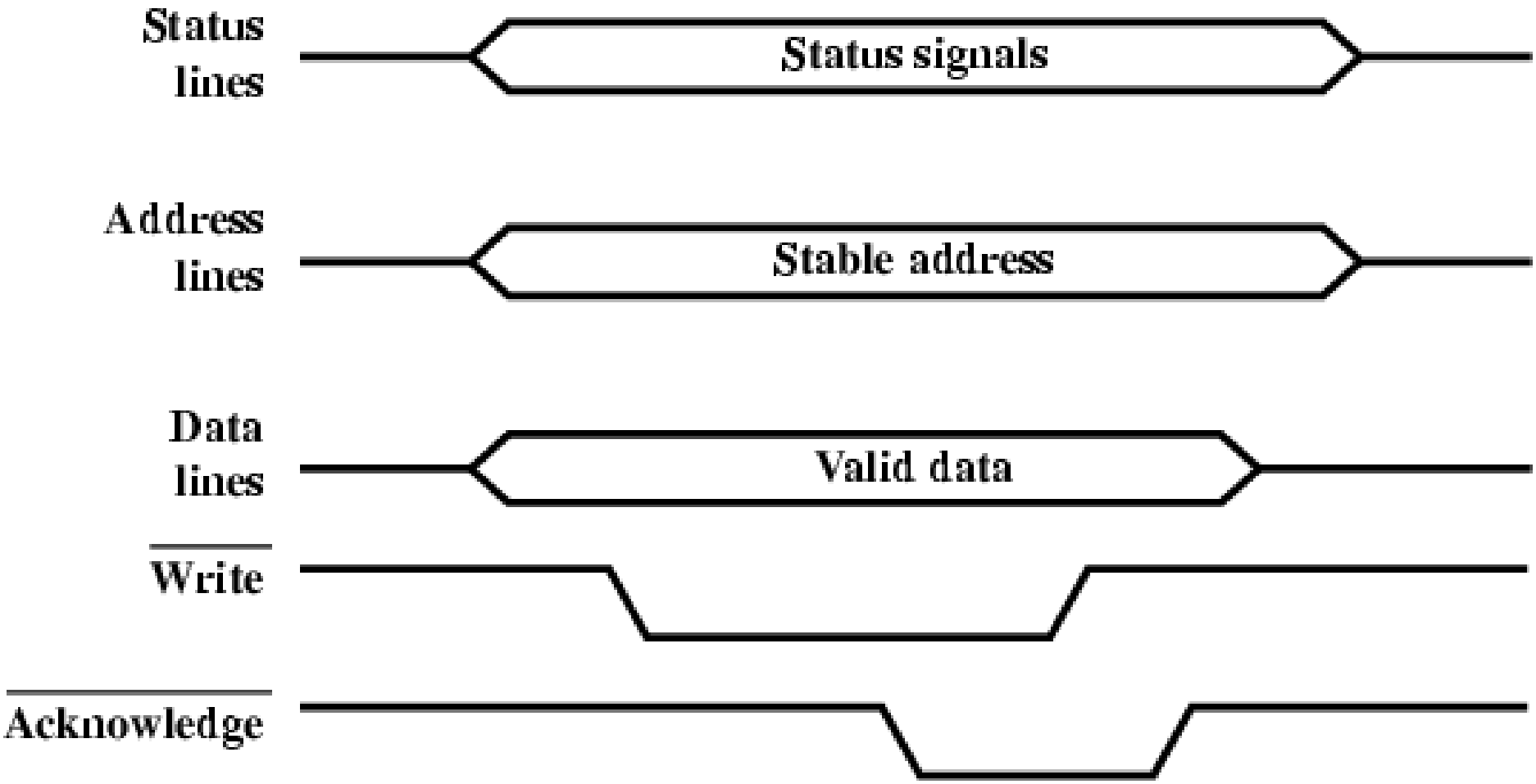
# Synchronous Timing Diagram



# Asynchronous Timing – Read Diagram



# Asynchronous Timing – Write Diagram



# Esempi : BUS PCI

# PCI Bus

- Peripheral Component Interconnection
- Intel released to public domain
- 32 or 64 bit
- 50 lines

# PCI Bus Lines (required)

- Systems lines
  - Including clock and reset
- Address & Data
  - 32 time mux lines for address/data
  - Interrupt & validate lines
- Interface Control
- Arbitration
  - Not shared
  - Direct connection to PCI bus arbiter
- Error lines

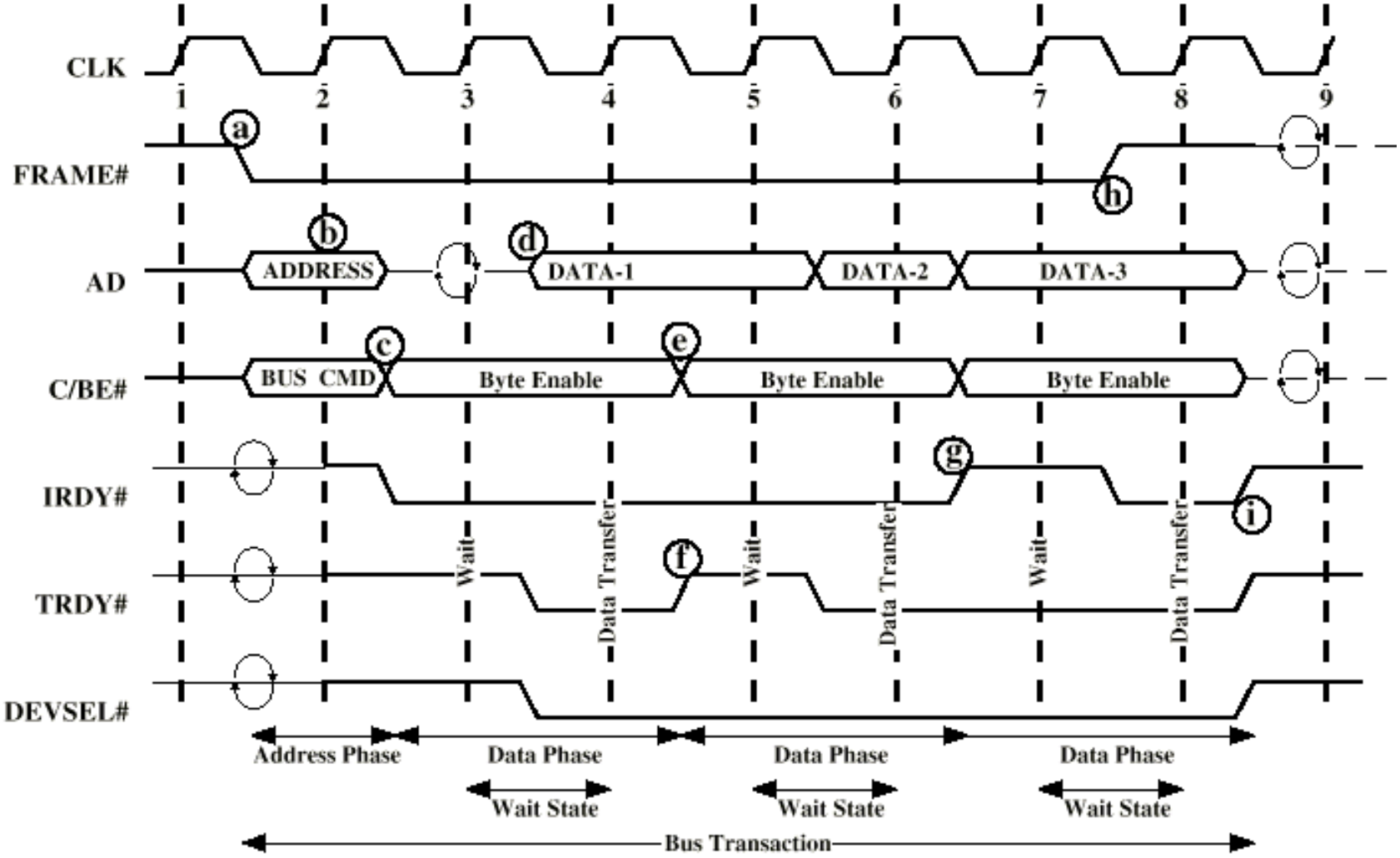
# PCI Bus Lines (Optional)

- Interrupt lines
  - —Not shared
- Cache support
- 64-bit Bus Extension
  - —Additional 32 lines
  - —Time multiplexed
  - —2 lines to enable devices to agree to use 64-bit transfer
- JTAG/Boundary Scan
  - —For testing procedures

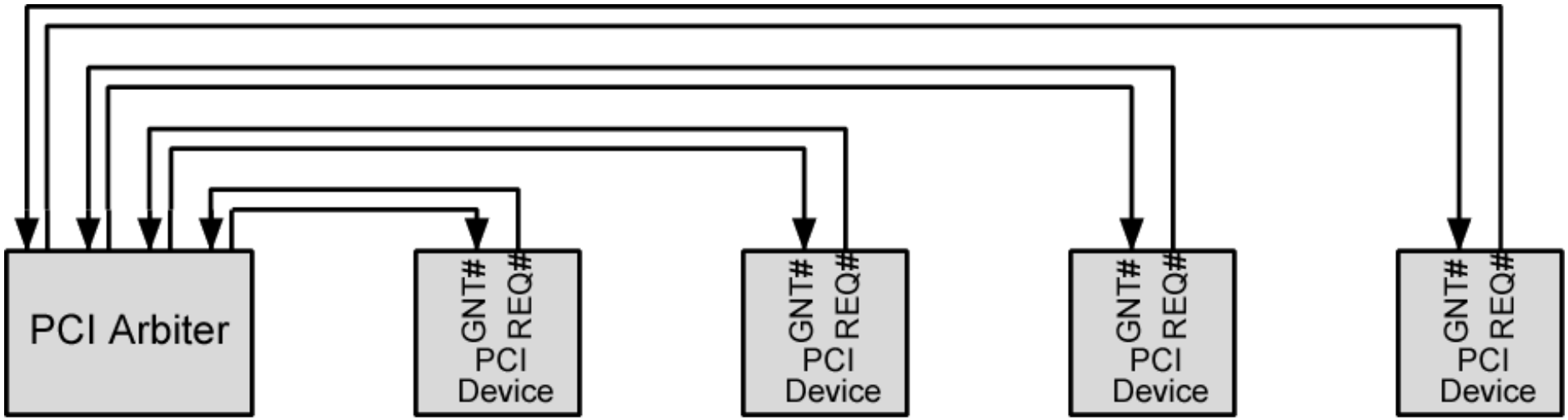
# PCI Commands

- Transaction between initiator (master) and target
- Master claims bus
- Determine type of transaction
  - e.g. I/O read/write
- Address phase
- One or more data phases

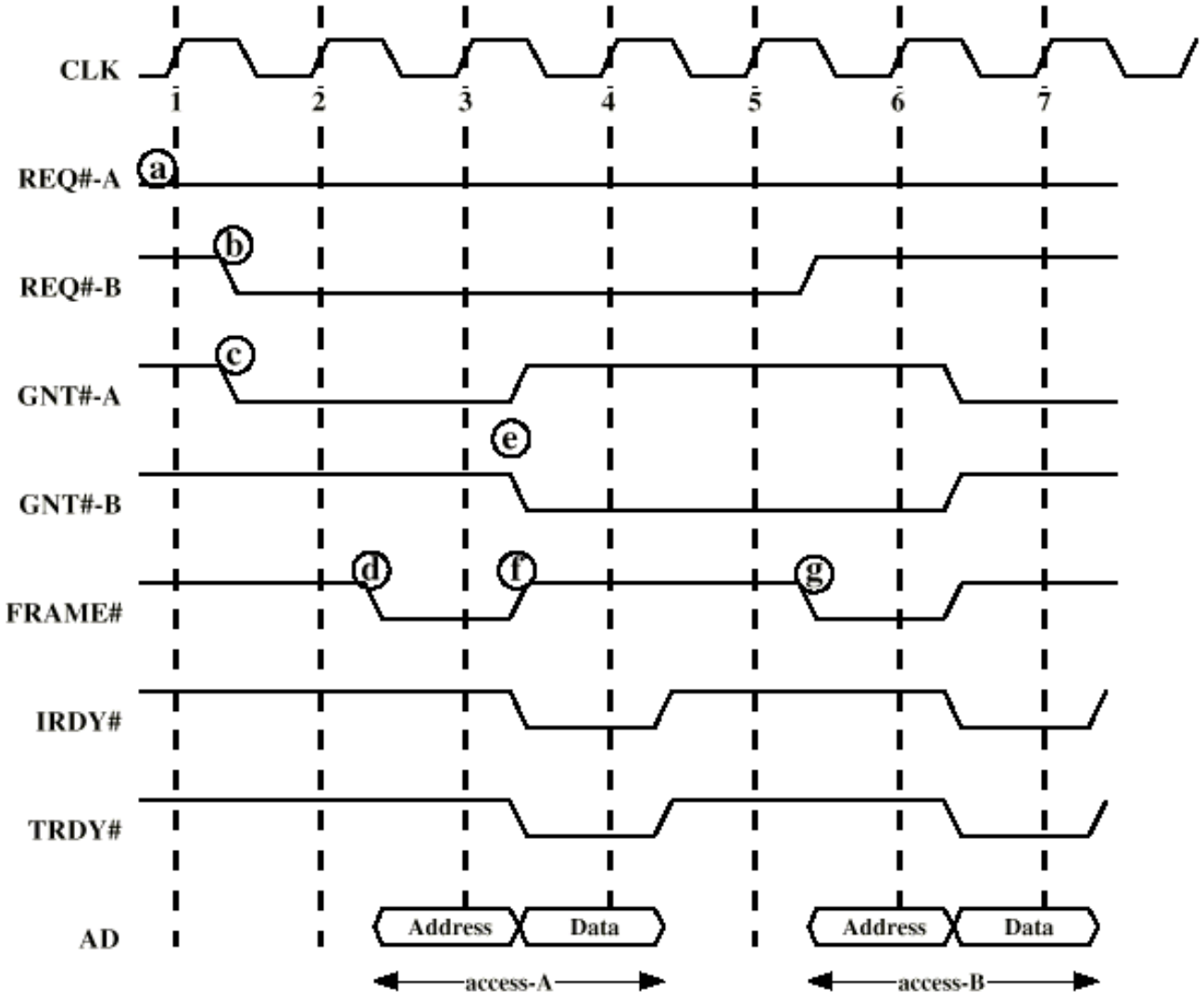
# PCI Read Timing Diagram



# PCI Bus Arbiter



# PCI Bus Arbitration



# Foreground Reading

- Stallings, chapter 3 (all of it)
- www.pcguide.com/ref/mbsys/buses/

- In fact, read the whole site!
- www.pcguide.com/